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04may04 14:27:01 User267149 Session D1373.1

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Alerts have been run.  See HELP NEWS 347 for details.
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  File 371:French Patents 1961-2002/BOPI 200209
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*File 371: This file is not currently updating. The last update is 200209.
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Set	Items	Description
S1	2618974	SEMICONDUCT?
S2	18206733	SUBSTRAT? OR SURFACE? OR BASE? OR SUBSTRUCT? OR UNDERSTRUC-T? OR UNDERLAY? OR FOUNDATION?
S3	9012843	PANE? OR DISK? OR DISC? OR WAFER?
S4	255203	CC=(A6855 OR A8115 OR B0520 OR B2570) OR MC=(T03-A01B OR T-03-A01B1) OR IC=G11B-005/704
S5	221787	HIGH????()(VOLT? OR POTENTIAL?)
S6	401823	(SILICON OR SI)(3N)(LAYER??? OR FILM??? OR COAT??? OR MULT-ILAYER??? OR MULTI()LAYER????? OR SPACER??? OR INTERLAYER???? OR INTER()LAYER????? OR MULTIPLE()LAYER? ?)
S7	2085319	(TOP OR UPPER OR BURIED OR DIELECTRIC?????? OR INTERPOS???-???? OR OXIDE OR INSULAT? OR THIN)(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR MULTI()LAYER????? OR SPACER??? OR INTERLAYER???? OR INTER()LAYER????? OR MULTIPLE()LAY...
S8	142408	(BODY OR SOURCE OR DRIFT)(3N)REGION? ?
S9	41190	BREAKDOWN()(VOLT? OR POTENTIAL?)
S10	1149720	S1 AND S2
S11	220964	S10 AND S3
S12	13740	S11 AND S4
S13	76	S12 AND S5
S14	16	S13 AND S6
S15	16	RD (unique items)
S16	60	S13 NOT S14
S17	17	S16 AND S7
S18	0	S17 AND S8
S19	1	S17 AND S9
S20	16	S17 NOT S19
S21	16	RD (unique items)
S22	43	S16 NOT S17
S23	1	S22 AND S8
S24	42	S22 NOT S23
S25	3	S24 AND S9
S26	3	RD (unique items)
S27	243732	S6 AND S7
S28	1820	S27 AND S5
S29	1820	S28 AND S7
S30	189	S29 AND S8
S31	48	S30 AND S9
S32	35	S31 AND S1
S33	33	RD (unique items)
S34	33	S33 NOT S14,S19,S23,S25
S35	28	S34 AND (S2 OR S3 OR S4)

15/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7463730 INSPEC Abstract Number: B2003-01-2550G-079
Title: Preparation of high aspect ratio 70 nm patterns by supercritical drying technique in proximity X-ray lithography
Author(s): Kikuchi, Y.; Fukuda, T.; Shishiguchi, S.; Masuda, K.; Kawakami, N.
Author Affiliation: Adv. Mater. & Process Technol. Lab., NTT Telecommun. Energy Labs., Kanagawa, Japan
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.4688, pt.1-2 p.896-902
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 2002 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(2002)4688:1/2L.896:PHAR;1-O
Material Identity Number: C574-2002-274
U.S. Copyright Clearance Center Code: 0277-786X/02/$15.00
Conference Title: Emerging Lithographic Technologies VI
Conference Sponsor: SPIE
Conference Date: 5-7 March 2002 Conference Location: Santa Clara, CA, USA
Language: English
Abstract: Supercritical drying (sc-drying) was applied for photoresist (resist) patterns replicated by proximity X-ray lithography. By that technique, 70 nm L/S patterns with an aspect ratio of 5 were successfully obtained without pattern collapse for both solvent and aqueous development resists by ZEP and UV6, respectively. The procedure was that a puddle developed 8 inch **wafer** was rinsed 3 times successively without spin drying by changing rinse liquids, and the **wafer**, wet with the 3rd rinse solution, which is soluble in supercritical CO/sub 2/, was transferred to a sc-drying chamber. The sc-drying process was performed under conditions of 8 MPa and 55 degrees C for about 15 min. The process uniformity within the **wafer** was examined by measuring the pattern width of 100 nm L/S with the resist UVII-HS and it was quite satisfactory. The feasibility study of dry etching with the sc-dried resist was performed. No noticeable change was found in etching ratio between **wafers** with/without sc-dried resist. The composition change of resist was also investigated by thermal desorption spectroscopy (TDS) and by molecular weight dispersion measurement, and no change was found after sc-drying. The sc-drying technique has **high potential** for acceptance in **semiconductor** device manufacturing.
Subfile: B

15/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

7074081 INSPEC Abstract Number: A2001-23-6855-023, B2001-12-0580-001
Title: Porous SiC **substrate** materials for high-quality epitaxial and bulk growth
Author(s): Mynbaeva, M.; Savkina, N.; Zubrilov, A.; Seredova, N.; Scheglov, M.; Titkov, A.; Tregubova, A.; Lebedev, A.; Kryzhanovski, A.; Kotousova, I.; Dmitriev, V.
Author Affiliation: A.F. Ioffe Phys. Tech. Inst., St. Petersburg, Russia
Conference Title: Substrate Engineering - Paving the Way to Epitaxy.

r Y

Symposium (Materials Research Society Symposium Proceedings Vol.587) p. O8.6.1-6
Editor(s): Norton, D.; Schlom, D.; Newman, N.; Matthiesen, D.
Publisher: Mater. Res. Soc, Warrendale, PA, USA
Publication Date: 2000 Country of Publication: USA viii+208 pp.
ISBN: 1 55899 495 5 Material Identity Number: XX-2000-02845
Conference Title: Substrate Engineering - Paving the Way Epitaxy. Symposium
Conference Date: 29 Nov.-3 Dec. 1999 Conference Location: Boston, MA, USA
Language: English
Abstract: The main unsolved problem in SiC technology is a high density of defects in **substrate** materials (micropipes and dislocations) propagating into device structures and causing device failure. Recently, significant progress in defect density reduction in **semiconductor** materials has been achieved using epitaxial lateral overgrowth techniques. In this paper, we describe a novel technique, which shows a **high potential** for defect reduction in epitaxial and bulk SiC. This technique is **based** on nanoscale epitaxial lateral overgrowth (NELOG) method, which employs porous **substrate** materials. Usually, the pores are from 50 to 500 nm in size and epitaxial material overgrowing these pores, forms continues high quality layer. It is important that the NELOG method does not require any mask. This technique may be easily scaled for large area **substrates**. In this work, SiC layers were grown on porous SiC by sublimation method, which is widely used for both epitaxial and bulk SiC growth. Porous SiC **substrates** were formed by **surface** anodisation of SiC commercial **wafers**. It was shown that SiC layers grown on porous SiC **substrates** have smooth **surface** and high crystal quality. The **surface** of overgrown material was uniform and flat without any traces of porous structure. X-ray topography indicated significant defect density and stress reduction in SiC grown on porous material. Photoluminescence measurements showed a reduction of deep level recombination in SiC.
Subfile: A B

15/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

6884477 INSPEC Abstract Number: A2001-09-7340Q-009, B2001-05-2530F-018
Title: Silica **films** on **silicon** carbide: a review of electrical properties and device applications
Author(s): Raynaud, C.
Author Affiliation: INSA, CNRS, Villeurbanne, France
Journal: Journal of Non-Crystalline Solids Conference Title: J. Non-Cryst. Solids (Netherlands) vol.280, no.1-3 p.1-31
Publisher: Elsevier,
Publication Date: Feb. 2001 Country of Publication: Netherlands
CODEN: JNCSBJ ISSN: 0022-3093
SICI: 0022-3093(200102)280:1/3L.1:SFSC;1-O
Material Identity Number: J120-2001-004
U.S. Copyright Clearance Center Code: 0022-3093/2001/$20.00
Conference Title: 3rd Symposium on SiO/sub 2/ and Advanced Dielectrics
Conference Sponsor: Eur. Commission - Human Potentional Programme - High Level Sci. Conference; Region Provence Alpes Cote d'Azur; et al
Conference Date: 19-21 June 2000 Conference Location: Fuveau, France
Language: English
Abstract: This paper reviews the present knowledge on silica films

(SiO/sub 2/) on silicon carbide (SiC). First, the kinetics of thermal oxidation of SiC are described, and the effects of a great number of parameters (various SiC polytypes, **substrate** type, **substrate** orientation...) are **discussed**. Mainly, thermal oxides grown on SiC are close to stoichiometric silica and the oxidation rate depends on the terminal face of the SiC monocrystal. The next four sections **discuss** the electrical properties of the oxide, and of the oxide/SiC interface, and especially the effects of materials and technological process on the interface state density and the effective oxide charge, and the origins of the interface states are **discussed** in detail. Oxides grown on n-type SiC have electrical properties (in terms of dielectric strength, leakage currents, interface trap, and oxide charges) measured by means of metal-oxide-**semiconductor** (MOS) structures, similar to oxides grown on silicon. Until recently, p-type SiC MOS structures have had a large equivalent oxide charge and larger interface state densities in spite of many efforts, compared to silicon MOS structures. It seems nevertheless that recent studies have improved the SiO/sub 2//SiC interfacial quality. Aluminum, carbon and alkali species are the main suspected contaminants. Finally, the author presents the applications of oxide films in SiC-**based** devices: MOS capacitors and MOS field effect transistors (MOSFETs) for microelectronics, MOSFETs for power electronics, and some applications using silica layers as a passivation layer. In spite of a smaller than required carrier mobility in the inversion layer, MOS field effect transistors (MOSFETs) have been demonstrated to operate up to 650 degrees C and integrated circuits **based** on NMOS and PMOS technologies have been successfully operated up to 300 degrees C. Vertical power MOSFETs are also of importance but their performances are still limited by a specific on-resistance larger than device requirements. The effect of charges present in the oxide on the electrical properties of **high voltage** diodes is also briefly **discussed**.

Subfile: A B

15/3,AB/4 (Item 4 from file: 2)

DIALOG(R)File 2:INSPEC

5484821 INSPEC Abstract Number: B9703-2560R-026

Title: **High voltage**, high speed lateral IGBT in thin SOI for power IC

Author(s): Leung, Y.K.; Kuehne, S.C.; Huang, V.S.K.; Nguyen, C.T.; Paul, A.K.; Plummer, J.D.; Wong, S.S.

Author Affiliation: Center for Integrated Syst., Stanford Univ., CA, USA

Conference Title: 1996 IEEE International SOI Conference Proceedings (Cat. No.35937) p.132-3

Publisher: IEEE, New York, NY, USA

Publication Date: 1996 Country of Publication: USA xvi+171 pp.

ISBN: 0 7803 3315 2 Material Identity Number: XX96-03123

Conference Title: 1996 IEEE International SOI Conference Proceedings

Conference Sponsor: IEEE Electron Devices Soc

Conference Date: 30 Sept.-3 Oct. 1996 Conference Location: Sanibel Island, FL, USA

Language: English

Abstract: Summary form only given. A lateral IGBT (LIGBT) built in thin SOI with a breakdown voltage higher than 700 V is reported for the first time. SOI **wafers** have been considered superior to bulk **substrates** for power IC applications. There have been reports on using a linearly graded dopant profile in the drift regions of PIN diodes and LDMOS devices in ultra-thin (<0.2 mu m) SOI **substrates** to achieve

high breakdown voltages. Reports have also shown that LIGBTs built in thin SOI **substrates** have faster switching speed than bulk and thick SOI counterparts. In principle, by employing a linearly graded profile in the drift region of an LIGBT, one would expect a device with low forward drop, high breakdown voltage and fast switching speed, which is ideal for **high voltage** and high speed applications. However, the thickness of the SOI **layer** (T/sub **si**/) in these devices is very crucial. Too thin a T/sub si/ will lead to problems such as high forward voltage drop, incapability in high-side configuration and high latchup susceptibility. If T/sub si/ is too large, however, an unrealistically thick buried oxide has to be used for high breakdown voltages and a linearly graded drift region will be difficult to achieve due to the two-dimensional diffusion of dopants.

Subfile: B

15/3,AB/5 (Item 5 from file: 2)

DIALOG(R)File 2:INSPEC

5104274 INSPEC Abstract Number: A9524-8115H-081, B9512-0520F-152

Title: Principles for controlling the electronic quality of high-rate deposited a-**Si**:H **films**

Author(s): Suchaneck, G.; Blum, T.; Roehlecke, S.; Kottwitz, A.

Author Affiliation: Inst. of Semicond. Technol. and Microsyst., Dresden Univ. of Technol., Germany

Journal: Journal de Physique IV (Colloque) Conference Title: J. Phys. IV, Colloq. (France) vol.5, no.C5, pt.2 p.655-61

Publication Date: June 1995 Country of Publication: France

CODEN: JPICEI ISSN: 1155-4339

Conference Title: Tenth European Conference on Chemical Vapour Deposition

Conference Date: 10-15 Sept. 1995 Conference Location: Venice, Italy

Language: English

Abstract: By altering the plasma generation frequency, applying a magnetic field, changing the plasma regime from the low voltage alpha -regime where the dominant electron-energy gain mechanism is related to the sheath expansion, to the **high voltage** gamma -regime where the **discharge** is maintained by secondary electrons emitted by the electrodes under ion bombardment, or generating a highly excited low-pressure plasma in a helicon-type source the influence of the particle and energy flux to the **substrate** on the a-**Si**:H **film** electronic properties was investigated. Deposition rate simulation was performed regarding a radical source located at the sheath/plasma boundary. Radical losses due to diffusion and reactive collisions with gas molecules were taken into account.

Subfile: A B

15/3,AB/6 (Item 6 from file: 2)

DIALOG(R)File 2:INSPEC

03774185 INSPEC Abstract Number: A91003637

Title: TEM in-situ investigations of the crystallization behaviour of amorphous **silicon** thin **films**

Author(s): Reiche, M.; Hopfe, S.

Author Affiliation: Inst. fur Festkorperphys. und Elektronenmikroskopie, Akad. der Wissenschaften, Halle/Saale, East Germany

Journal: Ultramicroscopy vol.33, no.1 p.41-50
Publication Date: July 1990 Country of Publication: Netherlands
CODEN: ULTRD6 ISSN: 0304-3991
U.S. Copyright Clearance Center Code: 0304-3991/90/$03.50
Language: English
Abstract: The crystallization of amorphous **silicon** thin **films** deposited on SiO/sub 2/ layers was in situ studied in a **high-voltage** electron microscope. The layers, grown by the LPCVD technique, were heated up to temperatures between 600 and 750 degrees C for up to 70 minutes. The investigations have shown that the crystallization behaviour differs for undoped and phosphorus-doped **layers**. Amorphous deposited **silicon layers** contain small crystallites already after the doping process (implantation at room temperature) which grow parallel to (111) directions of the underlying silicon **substrate**. The most dominant morphology of the growing crystallites displays a needle-like shape; the ratio of the length (longitudinal axis) to the width is close to 2, independent of the doping. The pre-existing crystallites in the phosphorus-doped material influence the twin frequency in the crystallites. Respective reasons are **discussed** on the basis of the TEM results.
Subfile: A

15/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

03540779 INSPEC Abstract Number: A90022617, B90007789
Title: Silicon-on-insulator technology by Si-MBE
Author(s): Maeder, M.; Zehe, A.
Author Affiliation: Sektion Phys., Tech. Univ. Dresden, East Germany
Journal: Diffusion and Defect Data - Solid State Data, Part B (Solid State Phenomena) vol.6-7 p.533-8
Publication Date: 1989 Country of Publication: Liechtenstein
CODEN: DDBPE8 ISSN: 0377-6883
Conference Title: 3rd International Autumn Meeting Gettering and Defect Engineering in the Semiconductor Technology
Conference Sponsor: Acad. Sci. GDR; VEB Kombinat Mikroelektron.; Phys. Soc. GDR
Conference Date: 8-13 Oct. 1989 Conference Location: Garzau, East Germany
Language: English
Abstract: Epitaxial dielectric **films** on large **Si wafers** are attractive candidates in order to realize Si-on-insulator (SOI) structures to be used in ultra large scale integration circuits, radiation-hard and **high voltage** devices, as well as in three-dimensional integrated circuits. Molecular beam epitaxy is gathering increasing importance in the fabrication of epitaxial insulating films. The paper concerns the MBE-growth of CaF/sub 2/-**films** on single crystal **Si substrates**. Particular emphasis is laid on **surface** and interface properties, but also on electrical characteristics.
Subfile: A B

15/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

03113111 INSPEC Abstract Number: B88026013
Title: Silicon-to-silicon direct bonding and its applications
Author(s): Shinbo, M.

Author Affiliation: Res. & Dev. Center, Toshiba Ceramics Co. Ltd., Hadano, Japan
Journal: Journal of the Institute of Electronics, Information and Communication Engineers vol.70, no.6 p.593-5
Publication Date: June 1987 Country of Publication: Japan
CODEN: DJTGEB ISSN: 0373-6121
Language: Japanese
Abstract: Epitaxial equivalent structure with single crystal **layer** and SOI (**silicon** on insulator) **wafer** can be made easily by adhering two sheets of silicon **wafer** to each other directly or via oxide films. SOI technology has become highlighted as indispensable technology to develop highly pressure-resistive, reliable and high-speed 3-dimensional ICs. High grade epitaxial **wafer** has also been used in the field of power device development in order to meet with requirements of **high voltage** and large capacity. Toshiba Ceramics Co. has successfully developed the technology of total **surface** adhesion of silicon **wafers** under room temperatures by activating the silicon **surfaces**. The author describes the technology and its applications.
Subfile: B

15/3,AB/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

02690737 INSPEC Abstract Number: B86041875
Title: Use of zone-melting recrystallization to fabricate a three-dimensional structure incorporating power bipolar and field-effect transistors
Author(s): Geis, M.W.; Chen, C.K.; Mountain, R.W.; Economou, N.P.; Lindley, W.T.; Hower, P.L.
Author Affiliation: MIT Lincoln Lab., Lexington, MA, USA
Journal: IEEE Electron Device Letters vol.EDL-7, no.1 p.41-3
Publication Date: Jan. 1986 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
U.S. Copyright Clearance Center Code: 0741-3106/86/0100-0041$01.00
Language: English
Abstract: Three-dimensional (3-D) structures were fabricated incorporating power bipolar transistors in a Si **substrate** and metal-oxide-**semiconductor** field-effect transistors (MOSFETs) in an overlying **silicon**-on-insulator (SOI) **film** that was zone-melting recrystallized with a graphite strip heater. Both N-P-N and P-N-P bipolar transistors were used. The N-P-N devices exhibited no significant change in transistor characteristics after zone-melting recrystallization (ZMR), while the P-N-P devices showed a substantial reduction in breakdown voltage. The MOSFETs exhibited electron mobilities comparable to those in similar devices fabricated in single-crystal Si **wafers**. The bipolar transistor yield is approximately 90%. The unusually high device quality and yield for 3-D structures obtained by the ZMR technique demonstrates the feasibility of fabricating monolithic structures incorporating both logic functions and relatively high-current **high-voltage** power switches.
Subfile: B

15/3,AB/10 (Item 10 from file: 2)
DIALOG(R)File 2:INSPEC

02462672 INSPEC Abstract Number: A85066820, B85034527

Title: Microscopic morphology and photoelectric properties of glow **discharged Si**:H **films**
Author(s): Kuwagaki, M.; Sato, T.; Shirafuji, J.; Inuishi, Y.
Author Affiliation: Dept. of Electr. Eng., Osaka Univ., Japan
Journal: Technology Reports of the Osaka University vol.34, no.1759-1781 p.271-8
Publication Date: Oct. 1984 Country of Publication: Japan
CODEN: TROUAI ISSN: 0030-6177
Language: English
Abstract: The **substrate** temperature dependence of transport and other properties of glow-**discharged** hydrogenated amorphous **silicon films** has been studied in connection with morphological heterogeneity in the films. The electron drift mobility at room temperature increases exponentially with raising **substrate** temperature in association with the formation of a percolation path by the growth of small quasi-crystalline zones. On the other hand, the lifetime or deep-level-trapping time has a maximum at the **substrate** temperature of 200 degrees C. This behavior is in parallel to those of the ESR spin density and photoluminescence intensity. The existence of small quasi-crystalline zones is evident by AC conductivity measurement and in situ observation of the thermal annealing effect in **high-voltage** transmission electron microscopy.
Subfile: A B

15/3,AB/11 (Item 11 from file: 2)
DIALOG(R)File 2:INSPEC

02461679 INSPEC Abstract Number: A85062135, B85033444
Title: Dielectrically isolated thick **Si films** by lateral epitaxy from the melt
Author(s): Celler, G.K.; Robinson, McD.; Trimble, L.E.; Lischner, D.J.
Author Affiliation: AT&T Bell Labs., Murray Hill, NJ, USA
Journal: Journal of the Electrochemical Society vol.132, no.1 p. 211-19
Publication Date: Jan. 1985 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651
Language: English
Abstract: Dielectric isolation (DI) technology has been available for almost 20 years. It was first developed for low capacitance, high speed circuits, and was later adapted to radiation-hardened devices and for **high voltage** isolation. The conventional DI technology is expensive, and device yields are reduced by mechanical instability of the polycrystalline **substrates** . The authors review a novel approach to forming DI structures, **based** on recrystallization from the melt of thick **Si films** deposited over oxidized **Si wafers**, with a regular array of seeding windows opened in the isolation oxide. The recrystallized films are free of grain boundaries and subboundaries and contain few dislocations. Most important, the polycrystalline **substrates** and the associated **wafer** bow are eliminated.
Subfile: A B

15/3,AB/12 (Item 12 from file: 2)
DIALOG(R)File 2:INSPEC

02396785 INSPEC Abstract Number: A85027634, B85012113
Title: Thick films for dielectric isolation by lateral epitaxy from the

melt
Author(s): Celler, G.K.; Trimble, L.E.
Author Affiliation: AT&T Bell Labs., Murray Hill, NJ, USA
Conference Title: Energy Beam-Solid Interactions and Transient Thermal Processing Symposium p.567-77
Editor(s): Fan, J.C.C.; Johnson, N.M.
Publisher: North-Holland, New York, NY, USA
Publication Date: 1984 Country of Publication: USA xviii+791 pp.
ISBN: 0 444 00903 5
Conference Sponsor: U.S. Army Res. Office
Conference Date: 14-17 Nov. 1983 Conference Location: Boston, MA, USA
Language: English
Abstract: Dielectric isolation (DI) technology has been available for almost twenty years. It was first developed for low capacitance, high speed circuits, and was later adapted to radiation hardened devices and for **high voltage** isolation. The authors describe a new method of forming DI structures that simplifies **wafer** fabrication, reduces the density of process induced defects, and may lead to a more flexible device design. Their process is **based** on recrystallization from the melt of thick **Si films** deposited over oxidized **Si wafers**, with a regular array of seeding windows opened in the isolation oxide. The recrystallized films are free of grain boundaries and subboundaries.
Subfile: A B

15/3,AB/13 (Item 13 from file: 2)
DIALOG(R)File 2:INSPEC

01999442 INSPEC Abstract Number: A83023212, B83011803
Title: Microelectronics applications of deposited **Si films** recrystallized from the melt
Author(s): Celler, G.K.; Trimble, L.E.
Author Affiliation: Bell Labs., Murray Hill, NJ, USA
Journal: Journal de Physique Colloque vol.43, no.C-1 p.C1/353-62
Publication Date: Oct. 1982 Country of Publication: France
CODEN: JPQCAK ISSN: 0449-1947
Conference Title: CNRS International Colloquium on 'Polycrystalline Semiconductors'
Conference Date: 2-4 Sept. 1982 Conference Location: Perpignan, France
Language: English
Abstract: Crystalline **Si films** on insulating **substrates** are needed for high-performance large scale integrated circuits, for **high voltage** devices, and for large area circuits used in flat-**panel** displays. Such films have been successfully formed by selective melting and recrystallization of polycrystalline Si deposited from the vapor on oxidized Si **wafers** and on bulk fused silica. Depending on the precursor structure and on the melting procedure, large crystallites or single crystalline layers are achieved. The authors describe Si recrystallization with CW and Q-switched lasers, with graphite heaters and with high intensity lamps. Transistor fabrication in recrystallized films is reviewed, and the influence of residual grain boundaries and other defects on device performance is evaluated. In addition, applications of beam-processed polysilicon in conventional integrated circuits are described.
Subfile: A B

15/3,AB/14 (Item 14 from file: 2)
DIALOG(R)File 2:INSPEC

00378124 INSPEC Abstract Number: A72029708, B72013553
Title: Measurement of resistivity of epitaxial **wafers** using a voltage relaxation technique
Author(s): Agatsuma, T.
Author Affiliation: Hitachi Ltd., Kodaira, Tokyo, Japan
Journal: Journal of the Electrochemical Society vol.119, no.2 p. 237-44
Publication Date: Feb. 1972 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651
Language: English
Abstract: The steady-state value, V/sub s/, of the voltage relaxation characteristic which is observed when a **high- voltage** ramp is applied in the reverse direction to a point contact diode, is related to the resistivity of the epitaxial **wafer**. V/sub s/, measured on silicon slices, showed a power dependence of k/sub rho //sup n/ where rho is the resistivity of the silicon slice and k is a constant. This dependence was used to obtain calibration curves. It was also found that time spent in room air after epitaxial growth, and heat conduction from the back side of the **wafers** had to be taken into consideration. V/sub s/ could not be measured for approximately 1 hr after epitaxial growth, but after 2 or 3 hr it was possible to take stable measurements; this can be explained in terms of slow **surface** states which grow with the **silicon** dioxide **film**. When heat conduction from the back side of a **wafer** 200 mu thick is considered, it was found that the pulse width of the measuring voltage ramp should be less than 100 mu sec. If **wafers** were treated with hydrofluoric acid, then V/sub s/ could be measured immediately after such a treatment. However, when treatments were repeated on the same **wafer** and V/sub s/ was measured after every repetition, it was noted that V/sub s/ varied +or-4 to 5 V. It is suggested that the variation of V/sub s/ would be reduced if the fast **surface** states at the interface of the SiO/sub 2/ **film** and the **silicon** bulk could be fully occupied.
Subfile: A B

15/3,AB/15 (Item 15 from file: 2)
DIALOG(R)File 2:INSPEC

00319709 INSPEC Abstract Number: A71073732, B71037152
Title: Four-point-probe resistivity measurements on **silicon** heterotype epitaxial **layers** with altered probe order
Author(s): Severin, P.J.
Journal: Philips Research Reports vol.26, no.4 p.279-97
Publication Date: Aug. 1971 Country of Publication: Netherlands
CODEN: PRREA9 ISSN: 0031-7918
Language: English
Abstract: The four-point-probe method for resistivity measurements is applied to a thin, epitaxially grown, heterotype **silicon layer** with an imperfectly isolating junction to the well-conducting **substrate** . A bar-shaped structure is analysed for low-voltage operation, <kT/e, and for **high-voltage** operation as far as analytically possible. The more usual geometry of laterally infinite extent is dealt with in the low-voltage range and it is shown that both the sheet resistance and the interface-zero-bias resistance can be found from two four-point-probe measurements with altered probe order. The theory is substantiated with semi-quantitative experiments. It is advocated that four-point-probe measurements are done at millivolt level. The precision

and accuracy of four- point-probe measurements are **discussed**.
Subfile: A B

15/3,AB/16 (Item 16 from file: 2)
DIALOG(R)File 2:INSPEC

00225466 INSPEC Abstract Number: A71013199, B71007625
Title: Growth and characterization of ultra-thin epitaxial **silicon films**
Author(s): Yim, E.W.
Author Affiliation: Fairchild Camera Instrument Corp., Palo Alto, CA, USA
Conference Title: Electrochemical Society Fall meeting, extended abstracts p.439-40
Publisher: Electrochemical Soc, New York, NY, USA
Publication Date: 1970 Country of Publication: USA 539 pp.
Conference Sponsor: Electrochemical Soc
Conference Date: 4-8 Oct. 1970 Conference Location: Atlantic City, NJ, USA
Language: English
Abstract: A variety of devices, such as IMPATT diodes, JFET's, microwave transistors, ultra-**high voltage** npn mesa transistors, and high-gain, high-frequency NFET's, require good electrical ultra-thin epitaxial films having uniform thickness, uniform resistivity, and crystallographic perfection. Furthermore, the rapidly advancing device technology demands much tighter control of film thickness and resistivity in order to improve device yields and to optimize device characteristics. To meet these requirements, new technology must be developed because the present state-of-the-art process has been found inadequate to grow good-quality materials due to various reasons. Among them are CB shorts, low and soft breakdowns, and a large variation of both film thickness and resistivity. The extensive investigation into the two major areas causing these problems is **discussed**. They are: the entire epitaxial film and the film-**substrate** interface; in other words, the initial nucleation.

19/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

4705923 INSPEC Abstract Number: B9408-2570-014
Title: A new double epitaxial **layer dielectric** isolation technology for HVICs
Author(s): Narayanan, E.M.S.; Amaratunga, G.; Milne, W.I.
Author Affiliation: Dept. of Eng., Cambridge Univ., UK
p.113-18
Editor(s): Williams, R.K.; Baliga, B.J.
Publisher: IEEE, New York, NY, USA
Publication Date: 1993 Country of Publication: USA xviii+324 pp.
ISBN: 0 7803 1313 5
U.S. Copyright Clearance Center Code: 0 7803 1313 5/93/$3.00
Conference Title: Proceedings of ISPSD '93 - 1993 International Symposium on Power Semiconductor Devices and IC's
Conference Sponsor: IEEE; Inst. Electr. Eng. Japan
Conference Date: 18-20 May 1993 Conference Location: Monterey, CA, USA
Language: English
Abstract: A novel double epitaxial **layer dielectric** isolation (DELDI) technology suitable for **high-voltage** integrated circuits (HVICs) is presented. The application of the reduced **surface** field (RESURF) concept to enhance the **breakdown voltage** of a lateral double-diffused MOS (LDMOS) structure employing the DELDI technology is studied in detail. The **breakdown voltage** behavior of a DELDI structure is similar to that of an equivalent junction-isolated structure. The performances of various lateral power MOS controlled devices such as the LDMOS and lateral insulated gate bipolar transistors employing the DELDI technology are compared with those of their counterparts employing the conventional single layer DI technology. The performance of a lateral-emitter-switched thyristor structure using both technologies is examined. The performance of a new lateral-transistor-controlled thyristor is **discussed**.

21/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7467344 INSPEC Abstract Number: A2003-01-8115J-003
Title: Amorphous diamond-like carbon film prepared by shunting arc plasma-**based** ion implantation and deposition method
Author(s): Yukimura, K.; Xinxin Ma; Maruyama, T.; Kumagai, M.; Kohata, M.; Saito, H.
Author Affiliation: Dept. of Electr. Eng., Doshisha Univ., Kyotanabe, Japan
Conference Title: IEEE Conference Record - Abstracts. 2002 IEEE International Conference on Plasma Science (Cat. No.02CH37340) p.137
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2002 Country of Publication: USA 358 pp.
ISBN: 0 7803 7407 X Material Identity Number: XX-2002-01321
Conference Title: Proceedings of IEEE 29th International Conference on Plasma Sciences
Conference Sponsor: Plasma Sci. & Applictions Committee of the IEEE Nucl. & Plasma Sci. Soc
Conference Date: 26-30 May 2002 Conference Location: Banff, Alta., Canada
Language: English
Abstract: The shunting arc **discharge** is an alternating capacitor **discharge** through a rod of metal or semi-metal. An optimization of the **discharge** condition has realized the self-ignition of the arc **discharge** at a low input power to the rod, leading to a much longer lifetime of the rod compared with the conventional shunting arc and the peripheral arc. The shunting-arc-produced plasma mainly consists of metal or semi-metal ions, and it has also been demonstrated that the ions can be extracted from the plasma. Thus, the shunting arc can be used as pulsed ion sources of metal and semi-metal for plasma-**based** ion implantation and deposition (PBII-D). In this study, an amorphous diamond-like carbon film was prepared by PBII-D using a pulsed carbon shunting arc at pressure of 10/sup -3/ Pa. The morphology and characteristics of the film were measured by using XPS, XRD, and Raman spectroscopy. The plasma was generated by the release of the capacitor energy (20 mu F at a charging voltage of 1.2 kV) to serve into a carbon rod of 2 mm in diameter and 40 mm long. The carbon rod was held at each end by a pair of 10 * 10 mm square tungsten plates. The shunting arc current showed a damping oscillation with a peak current of 1.2 kA at 20 mu s. A negative **high voltage** pulse of -0.3 to 3 kV with a pulse width of 10 mu s and 20 kHz was repeatedly applied to the target of 80 mm in diameter, which was located at 40 mm away from the plasma source. The maximum film thickness was obtained at an applied voltage of around 1 kV. The XRD pattern indicated that the prepared film was amorphous. The XPS measurements showed that the film included tungsten. This means that the film of carbon-tungsten alloy can be prepared by the shunting arc system.
Subfile: A

21/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

7188165 INSPEC Abstract Number: A2002-07-8115J-003, B2002-03-0520X-029
Title: Formation of a-C **thin films** by plasma-**based** ion implantation
Author(s): Watanabe, T.; Yamamoto, K.; Koga, Y.; Tanaka, A.

Author Affiliation: Joint Res. Consortium of Frontier Carbon Technol., Japan Fine Ceramics Center, Nagoya, Japan
Journal: Science and Technology of Advanced Materials Conference Title: Sci. Technol. Adv. Mater. (UK) vol.2, no.3-4 p.539-45
Publisher: Elsevier,
Publication Date: Sept.-Dec. 2001 Country of Publication: UK
CODEN: STAMCV ISSN: 1468-6996
SICI: 1468-6996(200109/12)2:3/4L.539:FTFP;1-R
Material Identity Number: M853-2001-004
U.S. Copyright Clearance Center Code: 1468-6996/01/$20.00
Conference Title: Plasma Science Symposium 2001 jointed with the 18th Symposium of Plasma Processing
Conference Date: 24-26 Jan. 2001 Conference Location: Kyoto, Japan
Language: English
Abstract: Carbon films were prepared on a Si **wafer substrate** by using a plasma-**based** ion implantation (PBII) technique. The homogeneity of the carbon films formed on the three-dimensional object and the influence of the duty ratio of the pulse bias to the target on the property of the carbon films were investigated. The homogeneity of the carbon films formed on a convex face and that formed on a concave face by the incidence of the microwave to the target with a low angle of about -30 degrees was almost a constant. The application of the ECR plasma source, with a mirror field, to the PBII system was efficient enough to improve the homogeneity, even though the plasma density was not very high. Diamond-like carbon films with a flat **surface** and a low friction coefficient can be formed by applying negative **high-voltage** pulses to a **substrate** with a low duty ratio of 1%.
Subfile: A B
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21/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC
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7122074 INSPEC Abstract Number: A2002-03-6855-005
Title: Nanometric inversion domains in conventional molecular-beam-epitaxy GaN **thin films** observed by atomic-resolution **high-voltage** electron microscopy
Author(s): Iwamoto, C.; Shen, X.Q.; Okumura, H.; Matuhata, H.; Ikuhara, Y.
Author Affiliation: Sch. of Eng., Univ. of Tokyo, Japan
Journal: Applied Physics Letters vol.79, no.24 p.3941-3
Publisher: AIP,
Publication Date: 10 Dec. 2001 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951
SICI: 0003-6951(20011210)79:24L.3941:NIDC;1-8
Material Identity Number: A135-2001-050
U.S. Copyright Clearance Center Code: 0003-6951/2001/79(24)/3941(3)/$18.0
0
Language: English
Abstract: GaN films grown on sapphire **substrates** by conventional molecular-beam epitaxy were investigated by means of atomic-resolution **high-voltage** electron microscopy (ARHVEM). The atomic positions of Ga and N could be directly **discriminated** by ARHVEM to determine the polarity in GaN. It was revealed that N polarity GaN films possessed a high density of nanometric inversion domains (IDs) with Ga polarity. The ID boundary was constructed by an inversion and a c/2 translation, and formed fourfold and eightfold coordination along the boundary.
Subfile: A

21/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

5905579 INSPEC Abstract Number: A9811-7240-008, B9806-2560H-022
Title: Charge conduction process and photovoltaic effects in thiazole yellow (TY) **thin film based** Schottky devices
Author(s): Roy, M.S.; Sharma, G.D.; Gupta, S.K.
Author Affiliation: Camouflage Div., Defence Lab., Jodhpur, India
Journal: Thin Solid Films vol.310, no.1-2 p.279-88
Publisher: Elsevier,
Publication Date: 21 Nov. 1997 Country of Publication: Switzerland
CODEN: THSFAP ISSN: 0040-6090
SICI: 0040-6090(19971121)310:1/2L.279:CCPP;1-9
Material Identity Number: T070-98004
U.S. Copyright Clearance Center Code: 0040-6090/97/$17.00
Language: English
Abstract: The charge generation and photovoltaic effects observed with **thin films** of TY in the form of sandwich structures, were analysed by J-V, C-V and photoaction spectra. These measurements were explained in terms of n-type **semiconductivity** of TY **thin film** and by the formation of a Schottky barrier with ITO while Ohmic contact with an Al or In electrode. The existence of thermionic emission over the ITO-TY barrier has been observed in low voltage region, whereas at **high voltages**, the process is dominant by the series resistance of TY layer. Various electrical parameters were calculated from the analysis of J-V and C-V characteristics of the devices and **discussed** in details. The diode quality factor is higher for Al/TY/ITO than In/TY/ITO device which can be attributed to the formation of **thin layer** of Al/sub 2/O/sub 3/ between Al and TY. The photoaction spectra of the devices reveal that the fraction of light which is absorbed near the ITO-TY interface, to the depth of 180 AA, is responsible for producing the charge carriers. The photovoltaic parameters were also calculated from the J-V characteristics of the devices, under illumination and described in detail.
Subfile: A B

21/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

5894401 INSPEC Abstract Number: A9810-7360F-034, B9805-2520D-070
Title: Microstructure and opto-electronic properties of CdSe-**thin films**
Author(s): Klement, U.; Ernst, F.
Author Affiliation: Max-Planck-Inst. fur Metallforschung, Stuttgart, Germany
Conference Title: Polycrystalline Thin Films - Structure, Texture, Properties and Applications III. Symposium p.131-6
Editor(s): Yalisove, S.M.; Adams, B.L.; Im, J.S.; Zhu, Y.; Chen, F.R.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1997 Country of Publication: USA xiii+474 pp.
ISBN: 1 55899 376 2 Material Identity Number: XX98-00284
Conference Title: Polycrystalline Thin Films - Structure, Texture, Properties and Applications III. Symposium
Conference Date: 31 March-4 April 1997 Conference Location: San

Francisco, CA, USA
Language: English
Abstract: CdSe appears to be a promising material to replace amorphous hydrogenated silicon as the photosensitive part in the retina of the "Electronic Eye", a camera **based** on **thin film** technique.
We have investigated the influence of post-depositional annealing treatments with respect to the optimization of the photoconductive properties. TEM-, AFM- and XPS-measurements on CdSe **thin films** are reported. The formation of an oxide could not be detected by XPS-depth profiling of films annealed in air but chemisorption of oxygen is expected at the intergrain boundaries. Hence, **high potential** barriers for electron transport will be introduced. Under illumination, trapping of photo-generated holes will neutralize the charge at the intergrain boundaries leading to improved electric properties. However, the homogeneity of the photoconductive properties in CdSe is not yet satisfying. The formation of swellings and holes on the sample **surface** , found by AFM-measurements, can perhaps explain the inhomogeneity of the photoconductive properties. Using Si **wafers** as **substrate** material no improvement in texturing could be reached, since an amorphous CdSe-interlayer is formed.
Subfile: A B

21/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

5839828 INSPEC Abstract Number: A9807-8115J-004
Title: Characteristic features of an apparatus for plasma immersion ion implantation and physical vapour deposition
Author(s): Ensinger, W.; Klein, J.; Usedom, P.; Stritzker, B.; Rauschenbach, B.
Author Affiliation: Inst. fur Phys., Augsburg Univ., Germany
Journal: Surface and Coatings Technology Conference Title: Surf. Coat. Technol. (Switzerland) vol.93, no.2-3 p.175-80
Publisher: Elsevier,
Publication Date: Sept. 1997 Country of Publication: Switzerland
CODEN: SCTEEJ ISSN: 0257-8972
SICI: 0257-8972(199709)93:2/3L.175:CFAP;1-N
Material Identity Number: J630-98001
U.S. Copyright Clearance Center Code: 0257-8972/97/$17.00
Conference Title: Third International Workshop on Plasma-Based Ion Implantation
Conference Sponsor: Res. Center Rossendorf; Saxonian Ministr. Sci. & Arts ; AP & T Adv. Products & Technol.; et al
Conference Date: 15-18 Sept. 1996 Conference Location: Dresden, Germany
Language: English
Abstract: A coating apparatus that combines two material modification techniques, physical vapour deposition of a **thin film** and plasma immersion ion implantation, is described. The plasma is generated by an electron cyclotron resonance (ECR) microwave plasma source. In the upper part of the vacuum chamber, the plasma is confined in a magnetic field by means of a solenoid. In the lower part, a magnetron sputter cathode and a resistively heated evaporator are mounted, which are used for depositing **thin films** on the sample. The sample is clamped onto a water-cooled sample holder that can be moved in the vertical direction. It is connected to a novel **semiconductor-based high voltage** pulse generator that provides negative voltage pulses. The

characteristic features of this apparatus are presented, including technical data on the plasma source, pulse generator and deposition devices. Additionally, results on plasma characterization are **discussed** such as the ion density dependence on microwave power and gas pressure. Results on formation of TiN films by deposition of titanium and subsequent nitrogen PIII are presented.
Subfile: A

21/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

5686850 INSPEC Abstract Number: A9720-8115H-019, B9710-0520F-108
Title: Nitrogen plasma doping during metalorganic chemical vapor deposition of ZnSe
Author(s): Morimoto, K.; Kawamura, Y.; Inoue, N.
Author Affiliation: Res. Inst. for Adv. Sci. & Technol., Osaka Prefecture Univ., Japan
Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers, Short Notes & Review Papers) Conference Title: Jpn. J. Appl. Phys. 1, Regul. Pap. Short Notes Rev. Pap. (Japan) vol.36, no.7B p.4949-52
Publisher: Publication Office, Japanese Journal Appl. Phys,
Publication Date: July 1997 Country of Publication: Japan
CODEN: JAPNDE ISSN: 0021-4922
SICI: 0021-4922(199707)36:7BL.4949:NPDD;1-R
Material Identity Number: F221-97015
Conference Title: ICRP-3/SPP-14. 3rd International Conference on Reactive Plasmas and 14th Symposium on Plasma Processing
Conference Sponsor: Japan Soc. Appl. Phys
Conference Date: 21-24 Jan. 1997 Conference Location: Nara, Japan
Language: English
Abstract: Active nitrogen generated by low-frequency **high-voltage** plasma **discharge** was used at pressures on the order of 1 Torr. Using a technique of alternate growth and plasma doping, high-quality N-doped ZnSe layers were grown on GaAs(100) **substrates**. In the low-temperature photoluminescence (PL) spectra, the narrow and distinct peak for acceptor-bound exciton, together with donor-acceptor pair peaks is predominant, which suggests N-acceptor doping on the order of 10/sup 18/ cm/sup -3/. The strong PL intensity indicated that the layers were free from plasma damage. The successful doping at the relatively high pressures strongly suggests that the metastable state (A/sup 3/ Sigma /sub u//sup +/) of a nitrogen molecule is responsible for the N doping. Although as-grown layers are highly resistive, they are converted to p-type layers with a hole concentration of ~1*10/sup 15/ cm/sup -3/ upon rapid thermal annealing at 700 degrees C.
Subfile: A B

21/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

5006315 INSPEC Abstract Number: A9516-8160C-019, B9509-2550E-035
Title: Effect of electron beam irradiation on Si **surface** cleaning in ultrahigh-vacuum system
Author(s): Miura, H.; Ohtaka, K.; Shindo, D.
Author Affiliation: Gen. Electron. Res. & Dev. Center, Ricoh Co. Ltd.,

Miyagi, Japan
Journal: Japanese Journal of Applied Physics, Part 2 (Letters) vol.34, no.5A p.L573-6
Publication Date: 1 May 1995 Country of Publication: Japan
CODEN: JAPLD8 ISSN: 0021-4922
Language: English
Abstract: Effect of electron beam irradiation (15 kV) on Si **surface** cleaning prior to epitaxial growth in an ultrahigh-vacuum system was investigated. A CaF/sub 2/ film was epitaxially grown on the Si **surface**, and the interface was observed by **high-voltage** electron microscopy. Amorphous layers, which were observed in the interface prepared with conventional thermal treatment at 750 degrees C, became much smaller with electron beam irradiation after the thermal treatment. **Based** on the electron microscope observation, the effect of electron beam irradiation on Si **surface** cleaning was briefly **discussed**.
Subfile: A B

21/3,AB/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

4730560 INSPEC Abstract Number: B9409-1210-057
Title: Prospects of **high voltage** power ICs on thin SOI
Author(s): Nakagawa, A.; Yasuhara, N.; Omura, I.; Yamaguchi, Y.; Ogura, T.; Matsudai, T.
Author Affiliation: Toshiba Corp., Kawasaki, Japan
p.229-32
Publisher: IEEE, New York, NY, USA
Publication Date: 1992 Country of Publication: USA 1022 pp.
ISBN: 0 7803 0817 4
U.S. Copyright Clearance Center Code: 0 7803 0817 4/92/$3.00
Conference Title: Proceedings of IEEE International Electron Devices Meeting
Conference Sponsor: Electron Devices Soc. IEEE
Conference Date: 13-16 Dec. 1992 Conference Location: San Francisco, CA, USA
Language: English
Abstract: Silicon on Insulator technology is promising for **high voltage** power IC applications. The required SOI layer thickness can be reduced if a large portion of the applied voltage is sustained by the bottom **insulator layer** . Combination of SOI and trenches or LOCOS has merits of simplified device isolation and high device packing density. **Thin** SOI **layer** will realize high-speed switching in **high voltage** devices because of the smaller amount of stored carriers. **Substrate** bias influences on device characteristics and potentials of SOI technology are **discussed**.
Subfile: B

21/3,AB/10 (Item 10 from file: 2)
DIALOG(R)File 2:INSPEC

03815292 INSPEC Abstract Number: A91029782
Title: Superconducting Y-Ba-Cu **oxide thin films** formed by ion beam mixing
Author(s): Rauschenbach, B.
Author Affiliation: Acad. of Sci., Central Inst. for Nucl. Res., Dresden,

East Germany
Journal: Journal of the Less-Common Metals vol.164-165, pt.A p. 438-43
Publication Date: 15 Oct. 1990 Country of Publication: Switzerland
CODEN: JCOMAH ISSN: 0022-5088
U.S. Copyright Clearance Center Code: 0022-5088/90/$3.50
Conference Title: 1990 European Materials Research Society (E-MRS) Spring Meeting Symposium A 'High-T/sub c/ Superconductor Materials'
Conference Date: 29 May-1 June 1990 Conference Location: Strasbourg, France
Language: English
Abstract: Polycrystalline superconducting **thin films** of Y-Ba-Cu oxides have been prepared by vapour deposition of alternate layers of Y, Ba, and Cu, followed by oxygen or xenon ion beam induced mixing and short-time post-annealing at temperatures up to 800 degrees C. The samples were completely superconducting between 80 and 91 K. The mixed layers have been studied by **high-voltage** electron microscopy, scanning electron microscopy, energy dispersive X-ray analysis, Rutherford backscattering, Auger electron spectroscopy and measurement of resistance. The condition of preparation of thin Y-Ba-Cu **oxide films** is **discussed.** The topography of **surface** is characterized by rough and smooth grains. The orthorhombic phase is fragmented in fine twin lamellae parallel with the (110) plane.
Subfile: A

21/3,AB/11 (Item 11 from file: 2)
DIALOG(R)File 2:INSPEC

03401416 INSPEC Abstract Number: A89081387
Title: The effect of sputtered impurities on the deep ion-implanted p/sup +/n junction in silicon
Author(s): Zamastil, J.; May, J.
Author Affiliation: CKD Prague, Czechoslovakia
Journal: Nuclear Instruments & Methods in Physics Research, Section B (Beam Interactions with Materials and Atoms) vol.B39, no.1-4 p.370-1
Publication Date: March 1989 Country of Publication: Netherlands
CODEN: NIMBEU ISSN: 0168-583X
U.S. Copyright Clearance Center Code: 0168-583X/89/$03.50
Conference Title: 6th International Conference on Ion Beam Modification of Materials (IBMM '88)
Conference Date: 12-17 June 1988 Conference Location: Tokyo, Japan
Language: English
Abstract: The authors have noticed that the concentration profiles of **high voltage** p/sup +/n junctions are influenced by unknown impurities near the silicon **surface** . Si (111) float zone high resistivity **wafers** were implanted with doses of 5*10/sup 15/ cm/sup -2/ aluminium at 400 keV on the Balzers SCI 218 high current implanter. After the diffusion the impurity profiles were measured by spreading resistance probe. It is shown that a shallow second pn junction was formed. They have concluded that those impurities were sputtered phosphorus atoms from the **wafer** holders. This problem can be avoided by depositing a thin screen oxide. The described method can be used for studies of the memory effects of the equipment.
Subfile: A

21/3,AB/12 (Item 12 from file: 2)
DIALOG(R)File 2:INSPEC

03238615 INSPEC Abstract Number: B88063053
Title: Fluxless and substantially voidless soldering for **semiconductor** chips
Author(s): Mizuishi, K.; Tokuda, M.; Fujita, Y.
Author Affiliation: Hitachi Ltd., Tokyo, Japan
Conference Title: 1988 Proceedings of the 38th Electronics Components Conference (88CH2600-5) p.330-4
Publisher: IEEE, New York, NY, USA
Publication Date: 1988 Country of Publication: USA x+664 pp.
U.S. Copyright Clearance Center Code: 0569-5503/88/0000-0330$01.00
Conference Sponsor: IEEE; Electron. Ind. Assoc
Conference Date: 9-11 May 1988 Conference Location: Los Angeles, CA, USA
Language: English
Abstract: A soldering method for reliability fabricating a composite structure is presented. This method, which need not use flux, provides a substantially voidless layer of solder that has low thermal resistance and excellent mechanical strength. A detailed description of soldering procedure, which uses a square, washer-shaped solder preform, is given. The experimental results show that the voids in the solder layer were reduced to less than 5% in bonds of silicon chips with a size of 1 cm/sup 2/. When 3-in silicon **wafer** chips were used, a similar void reduction took place. Moreover, pure solder flowed into the vacant region within the preform in such a manner that the native **oxide film** at the **surface** of the preform was removed. This resulted in an average solder bond shear strength that was greater than that obtained in the conventional manner using flux. The method was successfully applied to the fabrication of a multichip module. It was also used to make a **high-voltage** diode composed of ten silicon chips piled up vertically and connected with solder.
Subfile: B

21/3,AB/13 (Item 13 from file: 2)
DIALOG(R)File 2:INSPEC

02619401 INSPEC Abstract Number: A86040754
Title: Production of large vaporized metal clusters and their applications to functional metallurgical coatings
Author(s): Takaoka, H.; Yamada, I.; Takagi, T.
Author Affiliation: Ion Beam Eng. Exp. Lab., Kyoto Univ., Japan
Journal: Journal of Vacuum Science & Technology A (Vacuum, Surfaces, and Films) vol.3, no.6 p.2665-9
Publication Date: Nov.-Dec. 1985 Country of Publication: USA
CODEN: JVTAD6 ISSN: 0734-2101
U.S. Copyright Clearance Center Code: 0734-2101/85/062665-05$01.00
Conference Title: Proceedings of the 12th International Conference on Metallurgical Coatings
Conference Sponsor: American Vacuum Soc.; American Soc. Metals; Int. Union Vacuum Sci.; et al
Conference Date: 15-19 April 1985 Conference Location: Los Angeles, CA, USA
Language: English
Abstract: Cluster formation mechanism with large vaporized metal clusters is **discussed** , and several specific applications of ionized cluster beam (ICB) to films of metallurgical interest are described. In the ICB deposition and epitaxy, the crystallographic, mechanical, electrical,

optical, and magneto-optical properties of the metal and intermetallic compound films can be controlled by adjusting the acceleration voltage and the electron current for ionization. Metal-**based** and intermetallic compound-**based** films with characteristic advantages are reported: Cu films with strong adhesion and high packing density, Cu-Ni alloy films with controllable crystal structure and high strain gage, CdTe-PbTe superlattice with very **thin** and **multilayered** structures, and Cd/sub 1-x/Mn/sub x/Te films with large Faraday rotation and controllable composition and crystallinity. Thus, the ICB technique is found to have a **high potential** and unique features as an emerging technique for functional film formation and **surface** modification.
Subfile: A

21/3,AB/14 (Item 14 from file: 2)
DIALOG(R)File 2:INSPEC

01312497 INSPEC Abstract Number: A79023610
Title: Low-density dislocation arrays at heteroepitaxial Ge/GaAs-interfaces investigated by **high voltage** electron microscopy
Author(s): Strunk, H.
Author Affiliation: Inst. fur Phys., Max-Planck-Inst. fur Metallforschung, Stuttgart, West Germany
Journal: Applied Physics vol.18, no.1 p.67-75
Publication Date: Jan. 1979 Country of Publication: West Germany
CODEN: APHYCC ISSN: 0340-3793
Language: English
Abstract: **High-voltage** electron microscopy in combination with a large-area thinning technique has been applied to **thin** epitaxial Ge **layers** on GaAs **substrates**. These layers exhibit 60 degrees misfit dislocations along the (110) directions parallel to the interface. Various dislocation reactions are evaluated from the electron micrographs, e.g. the formation of non-glissile 90 degrees dislocations from two nearly parallel 60 degrees dislocations and the annihilation reaction of two crossing 60 degrees dislocations with identical Burgers vectors. The latter reaction occasionally leads to a dislocation multiplication. The misfit dislocations in very **thin layers** (approximately 0.5 mu m thickness and a linear dislocation density of less than 100 dislocation lines/cm) tend to be arranged in groups rather than being equidistant. Consequences for the interpretation of X-ray topograms are **discussed**.
Subfile: A

21/3,AB/15 (Item 15 from file: 2)
DIALOG(R)File 2:INSPEC

01130499 INSPEC Abstract Number: B78001303
Title: Techniques for measuring the integrity of passivation overcoats on integrated circuits
Author(s): Kern, W.; Comizzoli, R.B.
Issued by: Nat. Bur. Stand., Washington, DC, USA
Publication Date: March 1977 Country of Publication: USA 105 pp.
Report Number: NBS-SP-400-31
Language: English
Abstract: Conventional test methods to evaluate the quality of glass passivation overcoats on **semiconductor** devices are generally

inadequate and/or destructive. Three new methods have been devised that overcome these problems: (I) Sequential selective chemical etching of metal/dielectric structures to detect buried, latent, or partial defects as a function of **dielectric layer** depth. (II) Electrophoretic cell decoration with UV phosphor particles suspended in an insulating liquid, the sample forming one electrode of the cell. (III) Electrostatic corona charging to deposit selectively **surface** ions from a **high voltage** DC **discharge** on the insulating **surfaces** of the sample, followed by placing of the charged sample in a suspension of charged carbon black particles in an insulating liquid; depending on the polarity of the ions the particles can be deposited on the insulator **surface** or at the defect sites. The practical benefits of the new test methods can be considerable in production and product control, with cost savings through early detection of production line defects and rapid corrective action.

Subfile: B

21/3,AB/16 (Item 16 from file: 2)

DIALOG(R)File 2:INSPEC

00238296 INSPEC Abstract Number: B71012156

Title: **Semiconducting** varnish coating on the slot exits of **high voltage** rotating machine windings

Author(s): Drewnik, K.

Journal: Przeglad Elektrotechniczny vol.46, no.12 p.516-20

Publication Date: Dec. 1970 Country of Publication: Poland

CODEN: PZELAL ISSN: 0033-2097

Language: Polish

Abstract: The principle of the protection of **high voltage** rotating machine windings slot exits against **surface discharges** by **semiconducting** varnish **layer** applied on the **insulation surface** is described. Different solutions of the protecting arrangement and the progress in materials used for protecting coating are **discussed.**

Subfile: B

23/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

03361415 INSPEC Abstract Number: B89030511
Title: Device design of a **high voltage** BiCMOS IC
Author(s): Qin-Yi Tong; Wei Wu
Author Affiliation: Microelectron. Center, Nanjing Inst. of Technol., China
Conference Title: Solid State Devices. Proceedings of the 17th European Solid State Device Research Conference, ESSDERC '87 p.211-14
Editor(s): Soncini, G.; Calzolari, P.U.
Publisher: North-Holland, Amsterdam, Netherlands
Publication Date: 1988 Country of Publication: Netherlands xxvi+1084 pp.
ISBN: 0 444 70477 9
Conference Date: 14-17 Sept. 1987 Conference Location: Bologna, Italy
Language: English
Abstract: A new **high voltage** (HV) npn bipolar transistor for HV BiCMOS ICs has been developed which is fully compatible with conventional low voltage n-well CMOS process. The npn transistor employs n-well of low voltage (LV) CMOS as the collector **drift region** and it acts as the self-isolation region as well. The narrow self-aligned **base** is a result of double diffusion. The device has shown a high performance, i.e. h/sub FE/ of 100, f/sub T/ of 31 MHz and BV/sub ceo/ of greater than 300 V. It is expected that complementary HV npn and pnp transistors of this type can be integrated with HV and LV CMOS and bipolar devices on a same chip by Si **wafer** direct bonding (SDB)/SOI technology.
Subfile: B

26/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7091546 INSPEC Abstract Number: B2001-12-1350H-069
Title: Development of a **high voltage** mmW GaAs PIN diode switch
Author(s): Hoag, D.; Curcio, D.; Boles, T.
Author Affiliation: M/A-COM, Tyco Electronics, Burlington, MA, USA
Conference Title: 2001 GaAs MANTECH Conference. Digest of Papers p. 141-4
Publisher: GaAs MANTECH, St.Louis, MO, USA
Publication Date: 2001 Country of Publication: USA 258 pp.
ISBN: 1 893580 02 4 Material Identity Number: XX-2001-00829
Conference Title: Proceedings of 2001 International Conference on Compound Semiconductor Manufacturing Technology
Conference Date: 21-24 May 2001 Conference Location: Las Vegas, NV, USA
Language: English
Abstract: The initial development of a three pole three throw, (3P3T), switch for 35 to 40 GHz applications on the **surface** was thought to be a straightforward frequency scaled adaptation of a previously completed 6 port, 77 GHz switch for automotive collision avoidance radar systems. This misimpression was clearly demonstrated during the customer funded development and reliability qualification of this switch. This paper covers the difficulties involved in transforming a relatively low voltage, system qualified and validated PIN switch product into a much higher voltage switch, 100% on **wafer** tested and characterized for all port characteristics at frequency with full reliability qualification. Topics covered include the techniques needed to increase the PIN switch **breakdown voltage** by modifying the PIN structure and incorporating nitride under the transmission lines. A description of the voltage limitations of this underlying nitride film and the use of test structures to validate the DC characteristics of the physical changes to the circuit dielectric structure along with the results of the final device high temperature qualification is provided. In addition, design and process changes to effect higher yields through reduced circuit element breakage, increased bond pad strength and improved metallization definition capability are **discussed.**
Subfile: B

26/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

4747857 INSPEC Abstract Number: B9410-2570-007
Title: Silicon-on-insulator devices for **high voltage** and power IC applications
Author(s): Arnold, E.
Author Affiliation: Philips Lab., Philips Electron. North America Corp., Briarcliff Manor, NY, USA
Journal: Journal of the Electrochemical Society vol.141, no.7 p. 1983-8
Publication Date: July 1994 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651
U.S. Copyright Clearance Center Code: 0013-4651/94/$5.00+0.00
Language: English
Abstract: Silicon-on-insulator (SOI) technology **based** on **wafer** bonding promises to deliver significant performance advantages

and cost reduction over the existing bulk silicon technologies used for making power integrated circuits. A review is presented of the fundamental considerations that arise in the study of SOI devices for **high-voltage** applications. Significant device design parameters, such as the off-state **breakdown voltage** on-state specific resistance, thermal dissipation, packing density, and manufacturability are **discussed** in the context of the applicable device physics and SOI material requirements. Several possible approaches for achieving high **breakdown voltages** in SOI devices are described. The advantages and limitations of each approach are **discussed** and illustrated with some recent results on experimental devices.

Subfile: B

26/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

03710812 INSPEC Abstract Number: B90061394

Title: Semi-insulating silicon nitride (SinSiN) as a resistive field shield

Author(s): Osenbach, J.W.; Knolle, W.R.
Author Affiliation: AT&T Bell Labs., Allentown, PA, USA

Journal: IEEE Transactions on Electron Devices vol.37, no.6, pt.1 p.1522-8
Publication Date: June 1990 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
U.S. Copyright Clearance Center Code: 0018-9383/90/0600-1522$01.00
Language: English

Abstract: A plasma-deposited semi-insulating silicon nitride (SinSiN) developed as a resistive sea passivation is **discussed.** Following a brief review of its properties, its use as a resistive sea is reviewed. It is shown that SinSiN can be used to improve the **breakdown voltage** of a **high-voltage** device by some 20 to 40 V by screening all **surface** charges. It is also shown that SinSiN provides device immunity to **surface** charges, thereby improving yield and reliability.

Subfile: B

35/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6913289 INSPEC Abstract Number: B2001-06-2560R-029
Title: Development of **high voltage thin film** SOI device with linearly doped **drift region**
Author(s): Zhang Sheng-Dong; Han Ru-Qi; Lai, T.; Sin, J.
Author Affiliation: Inst. of Microelectron., Beijing Univ., China
Journal: Acta Electronica Sinica vol.29, no.2 p.164-7
Publisher: Chinese Inst. Electron,
Publication Date: Feb. 2001 Country of Publication: China
CODEN: TTHPAG ISSN: 0372-2112
SICI: 0372-2112(200102)29:2L.164:DHVT;1-O
Material Identity Number: B902-2001-004
Language: Chinese
Abstract: Principle and method for designing **high voltage thin film** SOI devices with linearly doped **drift region** are given. LDMOS transistors are fabricated on the SOI **wafers** with **Si film** of 0.15 mu m and buried oxide of 2 mu m. The dependence of **breakdown voltages** of the **thin film** SOI devices on the concentration gradient in the linearly doped **drift region** is experimentally investigated for the first time. **Based** on the optimization of the impurity dose in **drift region,** the **breakdown voltage** over 612 V is observed in the SOI LDMOS transistors with 50 mu m **drift region.**
Subfile: B

35/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

03991234 INSPEC Abstract Number: B91069649
Title: A 100-V lateral DMOS transistor with a 0.3-micrometer channel in a 1-micrometer **silicon-film**-on-**insulator**-on-**silicon**
Author(s): Apel, U.; Graf, H.G.; Harendt, C.; Hofflinger, B.; Ifstrom, T.
Author Affiliation: Inst. fuer Mikroelektronik Stuttgart, Germany
Journal: IEEE Transactions on Electron Devices vol.38, no.7 p. 1655-9
Publication Date: July 1991 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
U.S. Copyright Clearance Center Code: 0018-9383/91/0700-1655$01.00
Language: English
Abstract: A novel LDMOS transistor structure with **breakdown voltages** above 100 V has been fabricated in silicon-on-insulator-on-silicon (SOIS). This structure has been fabrication by silicon direct bonding (SDB) and etch-back to a typical film thickness of 1 mu m. The **silicon** carrier **layer** (handle) serves as a back-gate electrode, which, under proper bias, improves the transistor characteristics significantly. The effective channel length or **basewidth** is 0.3 mu m. Under these conditions, the **drift region** becomes the current-limiting element. The physics in the **drift region** in **thin silicon films** (<or=1 mu m) in the transistor on-state is dominated by the injected electrons from the channel. The limitation of the maximum drain current is given by the quasi-saturation effect. Criteria for the further optimization of SOIS LDMOS transistors are presented.

Subfile: B

35/3,AB/3 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015911365
WPI Acc No: 2004-069205/200407
XRAM Acc No: C04-028706
XRPX Acc No: N04-055641
Wide-bandgap **semiconductor** device, for **high-voltage** application, comprises **drift** layer, **body region**, **source region**, and channel layer, each being made of wide bandgap **semiconductor** material
Patent Assignee: NISSAN MOTOR CO LTD (NSMO)
Inventor: HOSHI M; KANEKO S; SHIMOIDA Y; TANAKA H
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030201482	A1	20031030	US 2003410188	A	20030410	200407	B
JP 2003318410	A	20031107	JP 2002121807	A	20020424	200407	

Priority Applications (No Type Date): JP 2002121807 A 20020424
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030201482	A1		17	H01L-027/108	
JP 2003318410	A		8	H01L-029/80	

Abstract (Basic): US 20030201482 A1
Abstract (Basic):
NOVELTY - A wide-bandgap **semiconductor** device, e.g. field-effect transistor, comprises:
(i) a drift layer of first conductivity type, a **body region** of second conductivity type, a **source region** of first conductivity type, and a channel layer of first conductivity type, each being made of wide bandgap **semiconductor** material; and

(ii) a gate electrode having a **semiconductor** layer made of material with different bandgap energy from the wide bandgap material.
DETAILED DESCRIPTION - A wide-bandgap **semiconductor** device comprises:
(i) a drift layer (2) of first conductivity type;
(ii) a **body region** (3a, 3b) of second conductivity type disposed at the top **surface** of and in the drift layer;
(iii) a **source region** (4a-4d) of first conductivity type disposed at the top **surface** of and in the **body region**;
(iv) a channel layer (6a-6c) of first conductivity type disposed at the top of and in the **body region** adjacent to the **source region**, and at the top **surface** of and in the drift layer; and
(v) a gate electrode (8a-8c) including a **semiconductor** layer at the bottom so that the **semiconductor** layer is in direct contact with the **top surface** of channel **layer**.
The **drift** layer, **body region**, **source region**, and channel layer are made of wide bandgap **semiconductor** material. The **semiconductor** layer is made of **semiconductor** material having different bandgap energy from that of the wide bandgap **semiconductor** material.

An INDEPENDENT CLAIM is also included for fabrication of wide bandgap **semiconductor** device by forming a drift layer on **base** material made of wide bandgap **semiconductor** material; forming a **body region**, a **source region**, and a channel layer; depositing a **semiconductor** layer; and doping impurity atoms from the **top surface** of **semiconductor layer**.

USE - For **high-voltage** applications.

ADVANTAGE - The **semiconductor** device achieves miniaturization and has high **breakdown voltage**. A Schottky gate structure having a desired barrier height can be formed selectively and easily.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of the wide-bandgap **semiconductor** device.

Drift layer (2)
Body regions (3a, 3b)
Source regions (4a-4d)
Body contact **regions** (5a, 5b)
Channel layers (6a-6c)
Gate electrodes (8a-8c)
Drain electrode (9)
Source electrode (10)
pp; 17 DwgNo 1/4

35/3,AB/4 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015789267
WPI Acc No: 2003-851470/200379
Related WPI Acc No: 2001-071118; 2002-171492; 2002-188280
XRAM Acc No: C03-239779
XRPX Acc No: N03-679992

High voltage power MOSFET production, used for e.g. vehicle electrical system, involves diffusing portion of p-type **semiconductor** dopant from trenches, to adjacent portions of epitaxial layer

Patent Assignee: GEN SEMICONDUCTOR INC (GESE-N); BLANCHARD R A (BLAN-I)
Inventor: BLANCHARD R A
Number of Countries: 102 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020140025	A1	20021003	US 2000586407	A	20000602	200379	B
			US 200279945	A	20020220		
WO 200371585	A2	20030828	WO 2003US5211	A	20030220	200379	
US 6660571	B2	20031209	US 2000586407	A	20000602	200381	
			US 200279945	A	20020220		
AU 2003219831	A1	20030909	AU 2003219831	A	20030220	200427	

Priority Applications (No Type Date): US 200279945 A 20020220; US 2000586407 A 20000602

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020140025	A1		12	H01L-029/76	CIP of application US 2000586407
WO 200371585	A2	E		H01L-000/00	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SC SD SE SG SK SL TJ TM TN TR TT TZ UA UG UZ VC VN YU ZA ZM ZW
Designated States (Regional): AT BE BG CH CY CZ DE DK EA EE ES FI FR GB

GH GM GR HU IE IT KE LS LU MC MW MZ NL OA PT SD SE SI SK SL SZ TR TZ UG
ZM ZW

US 6660571	B2	H01L-021/332	CIP of application US 2000586407
			CIP of patent US 6593619
AU 2003219831	A1	H01L-029/76	Based on patent WO 200371585

Abstract (Basic): US 20020140025 A1
Abstract (Basic):

NOVELTY - A **silicon dioxide layer** is formed on the **surface** of the trenches in the **drift region** of the epitaxial **layer** (1). **Polysilicon** doped with p-type **semiconductor** dopant, is deposited over the **silicon dioxide layer**, to fill the trenches. A portion of the dopant is diffused from the trenches to adjacent portions of the epitaxial layer. A portion of the polysilicon is recrystallized to form single crystal silicon.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **high voltage** power MOSFET.

USE - For manufacturing **high voltage** power MOSFET (claimed) used in vehicle electrical system, power supply and in power management application.

ADVANTAGE - Enables to control the horizontal doped gradient accurately and enables to optimize the **breakdown voltage** and on-resistance of the MOSFET.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of the MOSFET.

Epitaxial layer (1)
Substrate (2)
Source regions (7, 8)
P-type regions (40, 42)
pp; 12 DwgNo 3/7

35/3,AB/5 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015626458
WPI Acc No: 2003-688629/200365
Related WPI Acc No: 2004-155003
XRAM Acc No: C03-188730
XRPX Acc No: N03-550194

Extended drain metal-oxide **semiconductor** device for **semiconductor** power integrated circuit device, includes lattice-type **drift region** formed in well region and comprising alternately arranged first and second lattices

Patent Assignee: ELECTRONICS & TELECOM RES INST (ELTE-N); KIM J D (KIMJ-I); LEE D W (LEED-I); PARK I Y (PARK-I); ROH T M (ROHT-I); YANG Y S (YANG-I)
Inventor: KIM J D; LEE D U; NOH T M; PARK I Y; YANG I S; LEE D W; ROH T M; YANG Y S
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030132459	A1	20030717	US 2002179492	A	20020624	200365	B
US 6617656	B2	20030909	US 2002179492	A	20020624	200367	
KR 2003062489	A	20030728	KR 20022695	A	20020117	200381	

Priority Applications (No Type Date): KR 20022695 A 20020117
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes

US 20030132459 A1   13 H01L-029/76
US 6617656   B2   H01L-029/78
KR 2003062489 A   H01L-029/78

Abstract (Basic): US 20030132459 A1
Abstract (Basic):

NOVELTY - An extended drain metal-oxide **semiconductor** device has a lattice-type **drift region** formed in a given region of well region in silicon **substrate.** The **drift region** comprises alternately arranged first and second lattices.

The device also includes a field **oxide film,** a drain **region,** a diffusion **region, source** and **source** contact **regions,** a gate electrode, a gate **insulating film,** a source electrode, a drain electrode, and an **insulating film.**

DETAILED DESCRIPTION - An extended drain metal-oxide **semiconductor** (EDMOS) device consists of:

(i) a well region (204) formed in a given region of a silicon **substrate** (201);

(ii) a lattice-type **drift region** (208) formed in a given region of well region, and comprising alternate first and second lattices (208a, 208b);

(iii) a field **oxide film** (209, 209a) formed on the **substrate** and overlapped with a portion of well region or a portion of well and **drift regions;**

(iv) a drain region (213) formed in a given **region** of **drift region;**

(v) a diffusion region (208c) formed below the drain region;

(vi) **source** and **source** contact **regions** (212, 214) formed in the well region;

(vii) a gate electrode (211) formed on silicon **substrate** of well region;

(viii) a gate **insulating film** (210) intervened between the gate electrode and silicon **substrate;**

(ix) a source electrode (216) connected to the **source** and **source** contact **regions** via a contact hole formed in an **insulating film** (215); and

(x) a drain electrode (217) connected to the drain region via a contact hole formed in the **insulating film.**

An INDEPENDENT CLAIM is also included for fabrication of EDMOS device by:

(a) forming a well region in silicon **substrate;**

(b) alternately implanting first impurity ions in given region of well region to form lattice-type **drift region;**

(c) forming field **oxide film** on given region of silicon **substrate;**

(d) implanting second impurity ions in the well region to control a threshold voltage;

(e) forming a gate **insulating film** and a **polysilicon film** on the **substrate** of well region, and patterning the **polysilicon film** to form a gate electrode;

(f) implanting third impurity ions in the well **region** and **drift region** to form **source**/drain **regions,** respectively;

(g) implanting fourth impurity ions in the well **region** to form a **source** contact **region** connected to the **source region;**

(h) forming an **insulating film** on an entire structure, and forming contact holes to expose the **source region,** drain **region** and gate electrode; and

(i) forming metal wires connected to the **source region**, drain **region** and gate electrode via the contact holes, respectively.

USE - For use in **semiconductor** power integrated circuit (IC) devices requiring **high voltage**, high speed and high performance; IC devices for controlling the power of automobile and motor; and IC devices for driving display and communication devices.

ADVANTAGE - The EDMOS device has high **breakdown voltage** and low on resistance.

DESCRIPTION OF DRAWING(S) - The figure is a perspective view of the EDMOS device.

Substrate (201)
Well region (204)
Drift region (208)
First and second lattices (208a, 208b)
Diffusion region (208c)
Field **oxide films** (209, 209a)
Gate **insulating film** (210)
Gate electrode (211)
Source and **source** contact **regions** (212, 214)
Drain region (213)
Insulating film (215)
Source electrode (216)
Drain electrode (217)
pp; 13 DwgNo 2/5

35/3,AB/6 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015592825
WPI Acc No: 2003-654980/200362
XRAM Acc No: C03-178916

High voltage semiconductor device having buried transistor and manufacturing method thereof

Patent Assignee: HYNIX SEMICONDUCTOR INC (HYNI-N)
Inventor: KIM Y G
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2003033810	A	20030501	KR 200165950	A	20011025	200362	B

Priority Applications (No Type Date): KR 200165950 A 20011025
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2003033810	A		1	H01L-029/772	

Abstract (Basic): KR 2003033810 A
Abstract (Basic):

NOVELTY - A **high voltage semiconductor** device having a buried transistor and a manufacturing method thereof are provided to be capable of reducing process difficulties due to the topology of a gate, and improving the degree of integration and operational characteristics.

DETAILED DESCRIPTION - An SOI(Silicon On Insulator) **substrate** (20) is formed by sequentially forming a **buried oxide layer**(12) and a **silicon layer**(13) on a **silicon substrate**(11). An isolation layer(22) connected with the **buried oxide layer** is formed on the predetermined

portion of the **buried oxide layer** for defining an active region. After forming a trench in the active region, a gate(29) is formed on the center portion of the trench and a **polysilicon spacer**(30) is formed at both sidewalls of the trench, simultaneously. At this time, the **polysilicon spacer** is used as a buffer, thereby increasing **breakdown voltage**. A **source** and drain **region**(27) are formed at both sides of the gate(29). An **interlayer dielectric**(31) is formed on the resultant structure. The first, second and third metal wiring(34a,34b,34c) are formed on the **interlayer dielectric** for contacting the gate, the **source** and drain **region**, respectively. At the time, a transistor is buried in the trench, so that difficulties caused by the topology of a common transistor are solved.

pp; 1 DwgNo 1/10

35/3,AB/7 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015544702
WPI Acc No: 2003-606858/200357
XRAM Acc No: C03-165191
XRPX Acc No: N03-483868

Dual gate oxide **high voltage semiconductor** device, e.g. lateral metal oxide **semiconductor** field effect transistor or diode, comprises second gate oxide formed over portion of first gate oxide

Patent Assignee: KONINK PHILIPS ELECTRONICS NV (PHIG)
Inventor: LETAVIC T J; SIMPSON M R
Number of Countries: 102 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030107087	A1	20030612	US 200115847	A	20011210	200357	B
WO 200350884	A1	20030619	WO 2002IB4895	A	20021120	200357	
AU 2002348845	A1	20030623	AU 2002348845	A	20021120	200420	

Priority Applications (No Type Date): US 200115847 A 20011210
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030107087	A1		7	H01L-031/62	
WO 200350884	A1	E		H01L-029/78	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SC SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VC VN YU ZA ZM ZW

Designated States (Regional): AT BE BG CH CY CZ DE DK EA EE ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SK SL SZ TR TZ UG ZM ZW

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
AU 2002348845	A1			H01L-029/78	Based on patent WO 200350884

Abstract (Basic): US 20030107087 A1
Abstract (Basic):

NOVELTY - A dual gate oxide **high voltage semiconductor** device (100) comprises a **buried oxide layer** formed over a **semiconductor substrate** (102), a **silicon layer** formed over the **buried oxide layer** (104), a **top oxide layer** formed over the silicon **layer**, a first gate **oxide** formed over the **silicon layer** adjacent the **top oxide**

layer, and a second gate oxide formed over a portion of the first gate oxide.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method for forming a dual gate oxide **high voltage semiconductor** device.

USE - Used as **high voltage semiconductor** device e.g. lateral MOSFET or diode.

ADVANTAGE - Optimizes **breakdown voltage** and specific-on-resistance. Doping in the silicon can be increased without increasing the magnitude of the vertical electric field.

DESCRIPTION OF DRAWING(S) - The figure shows an enlarged view of a **semiconductor** device having dual gate oxide.

Semiconductor device (100)
Substrate (102)
Buried oxide layer (104)
Silicon layer (106)
Top oxide layer (114)
Field plate (116)
First gate oxide (124)
Second gate oxide (128)
pp; 7 DwgNo 3/3

35/3,AB/8 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015460689
WPI Acc No: 2003-522831/200349
XRAM Acc No: C03-140492
XRPX Acc No: N03-414914

High voltage metal oxide **semiconductor** device including shallow trench isolations

Patent Assignee: LIANHUA ELECTRONICS CO LTD (LIAN-N); UNITED MICROELECTRONICS CORP (UNMI-N)
Inventor: LIU C
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030089960	A1	20030515	US 2001986930	A	20011113	200349	B
CN 1419298	A	20030521	CN 2002132194	A	20020826	200355	

Priority Applications (No Type Date): US 2001986930 A 20011113
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030089960	A1		7	H01L-021/8238	
CN 1419298	A			H01L-029/76	

Abstract (Basic): US 20030089960 A1
Abstract (Basic):

NOVELTY - A **high voltage** metal oxide **semiconductor** device comprises a **substrate**, shallow trench isolations (STI), a field **oxide layer**, a **drift region** of a second conductive type, a gate structure, first and second **source regions** of the second conductive type, and first and second drain regions of the second conductive type. The STIs define an active area formed in the **semiconductor** layer.

DETAILED DESCRIPTION - A **high voltage** metal oxide **semiconductor** (HVMOS) device (100) comprises a **substrate** (101), STIs (114), a field **oxide layer** (120), a **drift region** (118) of a second conductive type, a gate structure (122),

first and second **source regions** (128, 132) of the second conductive type, and first and second drain regions (130, 134) of the second conductive type. The **substrate** has a **semiconductor** layer (112) of a first conductive type on an **insulating layer** (110). The STIs define an active area (116) formed in the **semiconductor layer**. The field **oxide layer** is formed in the active area of the **semiconductor** layer. The **drift region** is formed under the field **oxide layer**. The gate structure is formed on the **semiconductor** layer in the active area to cover a portion of the field **oxide layer**. The first and second **source regions** have first and second dopant concentration, respectively. The first **source** and drain **regions** having first dopant concentration are formed opposite to each other aside of the gate structure. The first drain region is isolated from the gate structure by the field **oxide layer**. The second **source** and drain **regions** having a second dopant concentration are formed in the first **source region** and the first drain region, respectively. The second dopant concentration is higher than the first dopant concentration.

USE - Used as a HVMOS device.

ADVANTAGE - High junction **breakdown voltage** and smaller dimension. It eliminates the **substrate** current path.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of the **high voltage** metal oxide **semiconductor** (HVMOS) device during fabrication.

HVMOS (100)
Substrate (101)
Insulating layer (110)
Semiconductor layer (112)
STIs (114)
Active area (116)
Drift region (118)
Field **oxide layer** (120)
Gate structure (122)
Gate dielectric (124)
Conductive layers (126)
First and second **source regions** (128, 132)
First and second drain regions (130, 134)
pp; 7 DwgNo 1D/1

35/3,AB/9 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014419263
WPI Acc No: 2002-239966/200229
Related WPI Acc No: 1999-419182
XRPX Acc No: N02-185132

High voltage transistor for integrated circuits has initially wider **drift region** caused by offset doping profile and thinning of **semiconductor** on **insulator layer**

Patent Assignee: KONINK PHILIPS ELECTRONICS NV (PHIG); PHILIPS ELECTRONICS NORTH AMERICA CORP (PHIG)
Inventor: ARNOLD E; LETAVIC T J; SIMPSON M R; LETAVIC T; SIMPSON M
Number of Countries: 025 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200175980	A1	20011011	WO 2001EP3007	A	20010319	200229	B
US 6310378	B1	20011030	US 97998048	A	19971224	200229	

			US 2000539911	A	20000330	
KR 2002019047	A	20020309	KR 2001715312	A	20011129	200262
EP 1269548	A1	20030102	EP 2001915360	A	20010319	200310
			WO 2001EP3007	A	20010319	
TW 501266	A	20020901	TW 2001109915	A	20010425	200334
CN 1422442	A	20030604	CN 2001801463	A	20010319	200356
JP 2003529940	W	20031007	JP 2001573557	A	20010319	200370
			WO 2001EP3007	A	20010319	

Priority Applications (No Type Date): US 2000539911 A 20000330; US 97998048 A 19971224

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200175980	A1	E	32	H01L-029/78	

Designated States (National): CN JP KR
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6310378	B1			H01L-027/01	CIP of application US 97998048
KR 2002019047	A			H01L-029/78	
EP 1269548	A1	E		H01L-029/78	Based on patent WO 200175980

Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
TW 501266	A			H01L-027/01	
CN 1422442	A			H01L-029/78	
JP 2003529940	W		37	H01L-029/786	Based on patent WO 200175980

Abstract (Basic): WO 200175980 A1
Abstract (Basic):

NOVELTY - **Semiconductor** on insulator (SOI) device has doping profile and thinning of SOI layer offset allowing an segment (134) of the **drift region** (135) near the **source** (131) to be wider allowing greater current capacity.

DETAILED DESCRIPTION - An independent claim is also included for a method of fabricating the transistor. The **substrate** is topped by a **silicon layer** which has its resistance lowered with impurities. This is then appropriately treated with successive layers to form the transistor.

USE - Used as a **high voltage** transistor in integrated circuit devices.

ADVANTAGE - Transistor has improved current handling capability while maintaining an improved **breakdown voltage** capability.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section of the transistor.

Source region (131)
Offset region (134)
Drift region (135)
Drain region (136)
pp; 32 DwgNo 3/11

35/3,AB/10 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014416282
WPI Acc No: 2002-236985/200229
XRAM Acc No: C02-071664
XRPX Acc No: N02-182293

Making symmetrical **high voltage** metal oxide **semiconductor** transistor includes forming shallow trench isolations

on silicon-on-insulator **substrate**, and forming gate and two field oxides on active area

Patent Assignee: UNITED MICROELECTRONICS CORP (UNMI-N)

Inventor: LIU C

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6333234	B1	20011225	US 2001803886	A	20010313	200229	B

Priority Applications (No Type Date): US 2001803886 A 20010313

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6333234	B1		11	H01L-021/336	

Abstract (Basic): US 6333234 B1

Abstract (Basic):

NOVELTY - A symmetrical **high voltage** metal oxide **semiconductor** (HVMOS) transistor (201) is made by forming shallow trench isolations (STI) (106) on a silicon-on-insulator (SOI) **substrate** (100); forming a gate (118) and two field oxides (FOX) (108, 109) on the active area (105); forming two double diffuse drains (DDD) on the active area; and forming a drift area at the bottom of the FOX.

DETAILED DESCRIPTION - Making a symmetrical HVMOS on a **semiconductor wafer** comprises:

(a) forming STI and active area(s) on an SOI **substrate;**

(b) forming two unneighboring FOX on the active area;

(c) forming a gate between the FOX, with a portion of the gate covering the FOX;

(d) forming two first ion implantation areas and two second ion implantation areas on the **surface** of the active area not covered by the gate and the FOX; and

(e) forming two third ion implantation areas at the bottom of the FOX.

The first and second ion implantation areas are used to form two DDD, respectively, to function as source (114) and drain (116) regions of the HVMOS, while the third ion implantation areas are used as a drift area of the HVMOS.

USE - For making a symmetrical HVMOS transistor which is useful in electrical devices, e.g. central processing unit power supplies, power management systems, or alternating current/direct current converters.

ADVANTAGE - In contrast to prior method of forming HVMOS, the inventive method eliminates the **substrate** current path and decreases the **substrate** current. Further, it avoids the occurrence of the snap-back breakdown such that the snapback and **breakdown voltages** increase to improve the high reliability performance of the HVMOS transistor.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional schematic diagram of the HVMOS transistor on an SOI **substrate,** according to the inventive method.

SOI **substrate** (100)

Silicon **substrate** (101)

Insulation layer (102)

Single crystal **silicon layer** (104)

Active area (105)

STI (106)

FOX (108, 109)

Well (112)

Source region (114)

Drain region (116)

Gate (118)
HVMOS transistor (201)
pp; 11 DwgNo 2/11

35/3,AB/11 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014403916
WPI Acc No: 2002-224619/200228
Related WPI Acc No: 2002-370998
XRPX Acc No: N02-172084
Non-volatile **semiconductor** memory device, with partial-trench-isolation **insulating film** not reaching **buried oxide layer** in memory cell transistor
Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ)
Inventor: KUNIKIYO T; MAEDA S; MATSUMOTO T
Number of Countries: 005 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6314021	B1	20011106	US 2000715141	A	20001120	200228	B
DE 10064200	A1	20011220	DE 1064200	A	20001222	200228	
JP 2001351995	A	20011221	JP 2000171793	A	20000608	200228	
KR 2001110976	A	20011215	KR 20011159	A	20010109	200238	
TW 495903	A	20020721	TW 2001100425	A	20010109	200329	
KR 403257	B	20031030	KR 20011159	A	20010109	200417	

Priority Applications (No Type Date): JP 2000171793 A 20000608
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6314021	B1		45	G11C-007/00	
DE 10064200	A1			H01L-027/115	
JP 2001351995	A		26	H01L-021/8247	
KR 2001110976	A			H01L-027/115	
TW 495903	A			H01L-021/76	
KR 403257	B			H01L-029/788	Previous Publ. patent KR 2001110976

Abstract (Basic): US 6314021 B1
Abstract (Basic):
NOVELTY - In a memory cell transistor of a flash memory, a silicon **substrate** (2), **buried oxide layer** (BOX) (3), and **silicon layer** (4) form a **silicon** on insulator (SOI) **substrate** (1) in that order. In the upper **surface** of the **silicon layer** a partial-trench-isolation **insulating film** (5) is formed that does not reach the upper **surface** of the BOX layer.
DETAILED DESCRIPTION - In an element formation region defined by the partial-trench-isolation **insulating film**, inside the **upper surface** of the **silicon layer**, are a **source** and drain **region** paired with a **body region** (70) in between them. On the upper **surface** of the **silicon layer**, where the **body region** is formed, a multi layer structure, in which a gate **oxide film** (6), a floating gate (7), an **insulating film** (8) and a control gate (9) are layered in this order, constituting a gate electrode structure.
ADVANTAGE - The partial-trench-isolation **insulating film** is used instead of the conventional full-isolation

insulating film, to externally fix a potential of the **body region** through the **silicon layer** between the **upper surface** of BOX **layer** and partial-isolation **insulating film**. Therefore it is possible to avoid a malfunction caused by accumulation of the positive holes in the **body region** and enhance a **breakdown voltage** between the source and drain. As a result, a memory cell transistor which can perform write and read operations of data with a **high voltage**, is obtained.

It is also possible to enhance the source-drain **breakdown voltage**.

DESCRIPTION OF DRAWING(S) - A cross-section drawing of the structure of a memory cell transistor in a non-volatile **semiconductor** memory device is shown. Partial-trench-isolation **insulating film** (5)**silicon substrate** (2)buried **oxide layer** (3)**silicon layer** (4)SOI **substrate** (1)**body region** (70)gate **oxide film** (6)floating gate (7)**insulating film** (8)control gate (9)

pp; 45 DwgNo 1/50

35/3,AB/12 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014268093
WPI Acc No: 2002-088791/200212
XRAM Acc No: C02-027230
XRPX Acc No: N02-065385

Fabrication of **high-voltage** lateral double-diffused metal oxide **semiconductor** by electrically coupling electrical field shield conductive **layer** with gate conductive **layer** overlying field **oxide layer**

Patent Assignee: UNITED MICROELECTRONICS CORP (UNMI-N)
Inventor: YANG S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6306711	B1	20011023	US 98185398	A	19981103	200212	B

Priority Applications (No Type Date): US 98185398 A 19981103
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6306711	B1		10	H01L-021/336	

Abstract (Basic): US 6306711 B1
Abstract (Basic):

NOVELTY - A **high-voltage** lateral double-diffused metal oxide **semiconductor** is made by forming a field oxidation to form a field **oxide layer** in a first opening; and forming gate oxide, gate conductive and electrical field shield conductive layers over a **substrate**. The field shield conductive layer is electrically coupled with the gate conductive layer that overlies the field **oxide layer**.

DETAILED DESCRIPTION - Fabrication of a **high-voltage** lateral double-diffused metal oxide **semiconductor** (LDMOS) includes providing a **substrate** having a first **oxide layer**. A first N-type ion implantation is performed to form a first N-well (202) in the **substrate**. A second N-type ion

implantation is performed to form a second N-well (203) in the **substrate**. The first **oxide layer** is removed. A pad **oxide layer** and a **silicon** nitride **layer** are formed over the **substrate**. A first opening is formed in the pad **oxide layer** and the **silicon** nitride **layer**. It exposes a portion of the **substrate**, the first N-well, and the second N-well. A field oxidation is performed to form a field **oxide layer** (207) in the opening. A portion of the field oxide is located on the **substrate** and the other portion is located on the first and second N-wells. The **silicon** nitride **layer** and the pad **oxide layer** are removed. A gate **oxide layer**, a gate conductive layer (209), and an electrical field shield conductive layer (210) are formed over the **substrate**. A portion of the gate conductive layer is located on the field **oxide layer**. The electrical field shield conductive layer is electrically coupled with the gate conductive layer and is formed from the same structural layer as the gate conductive layer. It is used as an electrical field shield under **high voltage**. It is located on the field **oxide layer** without the first and second N-wells below. A first P-type ion implantation is performed to form a P-doped region (211) in the **substrate**. A portion of the P-doped layer is below the gate conductive layer. A third N-type ion implantation is performed to form N+ drain region (212) in the second N-well and N+ **source region** (213) in the P-doped region. A second P-type ion implantation is performed to form a P+-doped layer (214) in the P-doped layer which is beside the N=**source region**. An isolation layer having a second opening and a third opening is formed over the **substrate**. First and second conductive layers are formed over the **substrate**. The first and second conductive layers are formed from the same structural layer. The second opening is filled by the first conductive layer. The first conductive layer bridges over the field **oxide layer** having an electrical field shield conductive and without the first N-well below. The third opening is filled by the second conductive layer.

USE - For fabricating a **high-voltage** LDMOS.

ADVANTAGE - The method decreases the strength of the electrical field at the junction between the **drift region** and the channel. It increases the **breakdown voltage** of **high-voltage** LDMOS, thus making the devices work normally.

DESCRIPTION OF DRAWING(S) - The figure shows a top view of a **high-voltage** LDMOS layout.

First N-well (202)
Second N-well (203)
Field **oxide layer** (207)
Gate conductive layer (209)
Electrical field shield conductive layer (210)
P-doped region (211)
N+ drain region (212)
N+ **source region** (213)
P+-doped layer (214)
pp; 10 DwgNo 2/4

35/3,AB/13 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014233769
WPI Acc No: 2002-054467/200207

XRAM Acc No: C02-015449
XRPX Acc No: N02-040110
Formation of **high voltage** devices compatible with low voltage devices used as, e.g. output/input circuits, involves forming field oxide regions on N and P wells, and forming N-type doped regions in the P well through an N grade implantation
Patent Assignee: UNITED MICROELECTRONICS CORP (UNMI-N)
Inventor: YANG S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6306700	B1	20011023	US 2000633468	A	20000807	200207	B

Priority Applications (No Type Date): US 2000633468 A 20000807
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6306700	B1		12	H01L-021/38	

Abstract (Basic): US 6306700 B1
Abstract (Basic):

NOVELTY - **High voltage** devices compatible with low voltage devices are formed by providing N-field and P-field **regions** as **drift** and as isolation **regions** in an N well and P well regions, respectively; forming field oxide regions on the N and P wells; and forming N-type doped regions in the P well through an N grade implantation, prior to forming a gate **oxide layer** and a **polysilicon layer**.

DETAILED DESCRIPTION - Formation of **high voltage** devices compatible with low voltage devices, involves: forming on a **substrate** (200) an **oxide layer**, an N well (204), and a pad **oxide layer** and a silicon nitride **layer**; defining the pad **oxide layer** and the **silicon** nitride **layer** to expose the **substrate**; forming a P well (212) in the **substrate**; forming N-field regions in the P well as **drift regions** respectively covering a portion of a channel for an N well metal oxide **semiconductor** (NMOS) transistor in the P well, and as isolation regions in the N well that respectively neighbor with a **source**/drain **region** for a P well MOS transistor in the N well; forming field oxide regions (220) on the exposed portions of the **substrate**; forming an N doped region (216a-b, 218a-b, 222a-b, 232a-b) between two the field oxide **regions** for enclosing the **source**/drain **region** for the NMOS transistor; forming P-field regions (224a-b, 226a-b, 234a-b) in the N-well as **drift regions** that respectively cover a portion of channel for a PMOS transistor, and as isolation regions in the P well that respectively **underlay** the field oxide **regions** adjoining the **source**/drain **region**; forming a gate **oxide layer** (228) on the **substrate**; forming a polysilicon gate (230a-b) crossing the channel and a portion of the adjoining field oxide regions; and forming an N+ type and P+ type doped regions in the P well and N well as the **source**/drain **region** for the NMOS and PMOS transistors, respectively.

USE - The method is used for forming **high voltage** devices compatible with low voltage devices used in **semiconductor** devices as, e.g. output/input circuits, watcher circuits, or as high/low voltage-integrated devices, such as liquid crystal display for notebook, or electronic parts for watch.

ADVANTAGE - The method provides better doping profile for a snap-back voltage, and increases the **breakdown voltage**. It prevents vertical transportation of carriers to avoid formation of

parasitic bipolar junction transistor, while controlling hot carrier effect.

DESCRIPTION OF DRAWING(S) - The figure is a schematic cross-sectional view of a **high voltage** device formed by the method.

Substrate (200)
N well (204)
P well (212)
N-type doped region (216a-b, 218a-b, 222a-b, 232a-b)
Field oxide regions (220)
P-field regions (224a-b, 226a-b, 234a-b)
Gate **oxide layer** (228)
Polysilicon gate (230a-b)
pp; 12 DwgNo 6/6

35/3,AB/14 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013933497
WPI Acc No: 2001-417711/200144
XRAM Acc No: C01-126198
XRPX Acc No: N01-309512

Thin-film silicon-on-**insulator** device, especially a **high-voltage** power device, comprises a lateral transistor and a lateral **drift region** having a retrograde doping profile with respect to buried and **surface** insulation regions

Patent Assignee: KONINK PHILIPS ELECTRONICS NV (PHIG); PHILIPS ELECTRONICS NORTH AMERICA CORP (PHIG)
Inventor: EGLOFF R; LETAVIC T; SIMPSON M; WARWICK A M
Number of Countries: 029 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200137346	A1	20010525	WO 2000EP10614	A	20001026	200144	B
US 6313489	B1	20011106	US 99440767	A	19991116	200170	
EP 1147561	A1	20011024	EP 2000979518	A	20001026	200171	
			WO 2000EP10614	A	20001026		
KR 2001101506	A	20011114	KR 2001708861	A	20010713	200230	
TW 472342	A	20020111	TW 2000124971	A	20001124	200281	
JP 2003514400	W	20030415	WO 2000EP10614	A	20001026	200328	
			JP 2001537800	A	20001026		

Priority Applications (No Type Date): US 99440767 A 19991116
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200137346	A1	E	14	H01L-029/78	
Designated States (National): JP KR					
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
US 6313489	B1			H01L-033/00	
EP 1147561	A1	E		H01L-029/78	Based on patent WO 200137346
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
KR 2001101506	A			H01L-027/12	
TW 472342	A			H01L-021/76	
JP 2003514400	W		17	H01L-021/336	Based on patent WO 200137346

Abstract (Basic): WO 200137346 A1
Abstract (Basic):

NOVELTY - **Thin-film silicon**-on-**insulator** (SOI) device comprises a lateral transistor and a lateral **drift region** having a retrograde doping profile with respect to buried and **surface** insulation regions

DETAILED DESCRIPTION - Lateral **thin-film silicon**-on-**insulator** (SOI) device includes **substrate, buried insulating layer** and lateral transistor formed in SOI **layer** on the **buried insulating layer** having a source of first type formed in a **body region** of second type. Lateral **drift region** of first type is adjacent the **body region** and forms lightly-doped drain **region.** Lateral **drift region** has retrograde doping profile between buried and **surface** insulation regions.

The doping at a portion of the lateral **drift region** adjacent the **buried insulation layer** is greater than that adjacent the **surface insulation layer.** A drain contact of first type is provided laterally spaced from the **body region** by the **drift region.**

USE - The silicon-on-insulator device is used in **high-voltage** power devices.

ADVANTAGE - The retrograde doping profile in the **drift region** increases **breakdown voltage** and reduces ON resistance.

DESCRIPTION OF DRAWING(S) - The drawing shows a lateral **thin-film** SOI device.

Semiconductor substrate (22)
Buried insulating layer (24)
SOI layer (26)
Source region (28)
Body region (30)
Lateral **drift region** (32)
Drain contact (34)
Surface insulation region. (38)
pp; 14 DwgNo 1/1

35/3,AB/15 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013240170
WPI Acc No: 2000-412044/200035
XRPX Acc No: N00-308014

Lateral **thin film silicon**-on-**insulator** device, e.g. MOSFET for **high-voltage** application, has lateral **drift region** with graded doping profile

Patent Assignee: KONINK PHILIPS ELECTRONICS NV (PHIG); PHILIPS ELECTRONICS NORTH AMERICA CORP (PHIG)
Inventor: LETAVIC T; SIMPSON M
Number of Countries: 023 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200031776	A2	20000602	WO 99EP8616	A	19991103	200035	B
EP 1050071	A2	20001108	EP 99972779	A	19991103	200062	
			WO 99EP8616	A	19991103		
US 6232636	B1	20010515	US 98200110	A	19981125	200129	
KR 2001034356	A	20010425	KR 2000708095	A	20000725	200164	
TW 441111	A	20010616	TW 2000100884	A	20000120	200203	
JP 2002530882	W	20020917	WO 99EP8616	A	19991103	200276	
			JP 2000584511	A	19991103		

Priority Applications (No Type Date): US 98200110 A 19981125
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200031776	A2	E	11	H01L-021/00	

Designated States (National): JP KR
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1050071	A2	E		H01L-021/00	Based on patent WO 200031776

Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6232636	B1			H01L-027/01	
KR 2001034356	A			H01L-021/20	
TW 441111	A			H01L-027/12	
JP 2002530882	W		15	H01L-029/786	Based on patent WO 200031776

Abstract (Basic): WO 200031776 A2
Abstract (Basic):

NOVELTY - An **insulating layer** (24) and lateral **drift region** (32) are formed on a **substrate** (22). A **source region** (28) is formed on a **body region** (30). A gate electrode (36) is formed on a **drift region** and are separated by insulation **region** (38). The **drift region** has a graded lateral doping profile. The doping profile slope of the first **drift region** (32A) exceeds the doping profile slope (M1) of the second **drift region** (32B).

USE - E.g. MOSFET, for **high voltage** application.

ADVANTAGE - Operates in a **high voltage**, high-current environment, such as low on' resistance and high **breakdown voltage**, giving a MOSFET with favorable performance characteristics.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the SOI device.

Semiconductor substrate (22)
Insulating layer (24)
Source region (28)
Lateral **drift region** (32)
Drift regions (32A,32B)
Gate electrode (36)
Insulation region (38)
pp; 11 DwgNo 1/2

35/3,AB/16 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013217469
WPI Acc No: 2000-389343/200034
XRAM Acc No: C00-118414
XRPX Acc No: N00-291547

Metal oxide **semiconductor**-gated power device comprises units having a **body region** of a first conductivity type in a **semiconductor** layer of second conductivity type and doped regions of first conductivity type formed in **semiconductor** layer

Patent Assignee: STMICROELECTRONICS SRL (SGSA); SGS THOMSON MICROELTRN SRL (SGSA)
Inventor: FRISINI F; FRISINA F
Number of Countries: 027 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week

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EP 1009036     A1  20000614  EP 98830737     A   19981209  200034  B
JP 2000183348  A   20000630  JP 99349998     A   19991209  200037
US 6586798     B1  20030701  US 99457122     A   19991207  200345
US 20030201503  A1  20031030  US 99457122     A   19991207  200372
                             US 2003430771   A   20030506
```

Priority Applications (No Type Date): EP 98830737 A 19981209

Patent Details:

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Patent No  Kind Lan Pg   Main IPC    Filing Notes
EP 1009036    A1 E  13 H01L-029/78
   Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT
   LI LT LU LV MC MK NL PT RO SE SI
JP 2000183348 A      8 H01L-029/78
US 6586798    B1       H01L-029/76
US 20030201503 A1       H01L-029/76   Div ex application US 99457122
                                     Div ex patent US 6586798
```


Abstract (Basic): EP 1009036 A1

Abstract (Basic):

NOVELTY - Metal oxide **semiconductor** (MOS)-gated power device comprises a set of elementary functional units, each unit comprising a **body region** (3) of a first conductivity type formed in a **semiconductor** material layer (21, 22, 23) of a second conductivity type. A set of doped regions (201, 202) of a first conductivity type is formed in layer (21, 22, 23).

DETAILED DESCRIPTION - Each region (201, 202) is disposed under a respective region (3) and is separated from other doped regions by parts of layer (21, 22, 23).

An INDEPENDENT CLAIM is also included for a method of manufacturing a MOS-gated power device.

USE - MOS-gated power device e.g., metal oxide **semiconductor** field effect transistor (MOSFET).

ADVANTAGE - **High voltage** MOS-gated power device has a low output resistance.

DESCRIPTION OF DRAWING(S) - The diagram shows a cross section of a **high voltage** MOS-gated power device.

Substrate (1)
Body region (3)
Source region (4)
Oxide layer (5)
Polysilicon layer (6)
Insulating material **layer** (7)
Semiconductor material layer (21, 22, 23)
Doped regions (201, 202)
pp; 13 DwgNo 13/13

35/3,AB/17   (Item 15 from file: 350)

DIALOG(R)File 350:Derwent WPIX

013023019

WPI Acc No: 2000-194870/200017

XRPX Acc No: N00-144201

Lateral **thin film silicon**-on-**insulator** device has finger shaped **region** extending from **body region** into **drift region** for depleting a portion of **drift region** adjacent to **body region** in lateral direction

Patent Assignee: KONINK PHILIPS ELECTRONICS NV (PHIG); PHILIPS NORTH AMERICA CORP (PHIG)

Inventor: LETAVIC T; SIMPSON M
Number of Countries: 023 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6028337	A	20000222	US 98187874	A	19981106	200017	B
WO 200028601	A2	20000518	WO 99EP8237	A	19991027	200032	
EP 1044475	A2	20001018	EP 99953957	A	19991027	200053	
			WO 99EP8237	A	19991027		
KR 2001033905	A	20010425	KR 2000707480	A	20000706	200164	
TW 455934	A	20010921	TW 2000100875	A	20000120	200242	
JP 2002529936	W	20020910	WO 99EP8237	A	19991027	200274	
			JP 2000581699	A	19991027		

Priority Applications (No Type Date): US 98187874 A 19981106
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6028337	A		7	H01L-027/12	
WO 200028601	A2	E		H01L-029/786	

Designated States (National): JP KR
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1044475	A2	E		H01L-029/786	Based on patent WO 200028601

Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2001033905	A			H01L-029/786	
TW 455934	A			H01L-021/283	
JP 2002529936	W		17	H01L-029/786	Based on patent WO 200028601

Abstract (Basic): US 6028337 A
Abstract (Basic):

NOVELTY - SOI MOS transistor (20) consists of a **source region** (28), **body region** (30), lateral **drift region** (32), drain **region** (34), and a gate electrode (36) provided on a **semiconductor surface** area (26) sequentially. Finger shaped region (30A) is provided extending from **region** (30) into the **drift region** for depleting portion of the **drift region** adjacent to the **body region** in the lateral direction during operation. The **semiconductor surface** layer is formed on **buried insulating layer** (24) provided on **substrate** (22).

USE - For **high voltage** application such as **high voltage** power devices.

ADVANTAGE - Exhibits high performance in **high voltage** and high current environment and enhances operation parameters such as ON resistance and **breakdown voltage.**

DESCRIPTION OF DRAWING(S) - The figure shows simplified cross-sectional view of a lateral **thin film** SOI device.

SOI MOS transistor (20)
Substrate (22)
Insulating layer (24)
Semiconductor surface area (26)
Source region (28)
Body region (30)
Finger shaped region (30A)
Drift region (32)
Drain region (34)
Gate electrode (36)
pp; 7 DwgNo 1/6

35/3,AB/18 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012813432
WPI Acc No: 1999-619663/199953
XRAM Acc No: C99-180828
XRPX Acc No: N99-456982
High voltage semiconductor device fabrication
Patent Assignee: UNITED MICROELECTRONICS CORP (UNMI-N)
Inventor: TUNG M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5976923	A	19991102	US 98209366	A	19981208	199953	B

Priority Applications (No Type Date): US 98209366 A 19981208
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5976923	A		7	H01L-021/8238	

Abstract (Basic): US 5976923 A
Abstract (Basic):
NOVELTY - The process comprises forming first p and n wells in a **substrate**, forming a **silicon oxide layer** over the **substrate**, and forming a second p and n wells in the first p well and the first n well, respectively. The **silicon oxide layer** is removed and replaced by a second silicon **oxide layer** and a patterned **silicon** nitride **layer**. A number of p-type **drift regions** are formed within the second p wells within the first p well and the first n well, and a number of n type **drift regions** are formed within the first n well and the first p well. A field **oxide layer** is formed between remaining portions of the **silicon** nitride **layer**, and the **silicon** nitride **layer** and the second **silicon oxide layer** are removed. A gate **oxide layer** is formed and patterned by a mask which covers portions between every 2 adjacent p type **drift regions** and every 2 adjacent n type **drift regions**. A number of patterned polysilicon gates are formed on the gate **oxide layer**, and a number of n-type and p-type heavily doped regions are formed in the second n wells and p wells, respectively.

USE - Used for fabricating a **high voltage semiconductor** device.

ADVANTAGE - Current driving performance and latch-up capability are improved resulting in a reduced area being required for the device. **Breakdown voltage** is increased at the junctions between the **source**/drain **regions** and the **substrate**.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of the **high voltage** device.

n-type heavily doped **source**/drain **regions** (270)
n wells (220)
p-type heavily doped **source**/drain **regions** (280)
Substrate (200)
pp; 7 DwgNo 4F/4

35/3,AB/19 (Item 17 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011355135
WPI Acc No: 1997-333042/199730
XRPX Acc No: N97-276394
Lateral **thin-film semiconductor**-on-**insulator** for **high-voltage** and power applications - has linear lateral doping profile in lateral **drift region** and conductive field plate on linearly-graded **top oxide insulating layer**
Patent Assignee: KONINK PHILIPS ELECTRONICS NV (PHIG); PHILIPS ELECTRONICS NV (PHIG); PHILIPS NORDEN AB (PHIG); US PHILIPS CORP (PHIG)
Inventor: MERCHANT S L
Number of Countries: 020 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9722149	A1	19970619	WO 96IB1296	A	19961125	199730	B
US 5648671	A	19970715	US 95571486	A	19951213	199734	
EP 809864	A1	19971203	EP 96937463	A	19961125	199802	
			WO 96IB1296	A	19961125		
JP 11501163	W	19990126	WO 96IB1296	A	19961125	199914	
			JP 97521877	A	19961125		
KR 98702126	A	19980715	WO 96IB1296	A	19961125	199927	
			KR 97705521	A	19970811		
EP 809864	B1	20030709	EP 96937463	A	19961125	200353	
			WO 96IB1296	A	19961125		
DE 69629017	E	20030814	DE 629017	A	19961125	200361	
			EP 96937463	A	19961125		
			WO 96IB1296	A	19961125		

Priority Applications (No Type Date): US 95571486 A 19951213
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9722149	A1	E	11	H01L-029/423	
Designated States (National): JP KR					
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
US 5648671	A		5	H01L-029/78	
EP 809864	A1	E		H01L-029/423	Based on patent WO 9722149
Designated States (Regional): DE FR GB					
JP 11501163	W		14	H01L-029/861	Based on patent WO 9722149
KR 98702126	A			H01L-029/78	Based on patent WO 9722149
EP 809864	B1	E		H01L-029/423	Based on patent WO 9722149
Designated States (Regional): DE FR GB					
DE 69629017	E			H01L-029/423	Based on patent EP 809864
					Based on patent WO 9722149

Abstract (Basic): WO 9722149 A

The lateral **semiconductor** device is provided in a thin **semiconductor film** on a **thin buried** oxide. The buried oxide is provided on a **semiconductor substrate**. The **semiconductor** device structure includes at least two **semiconductor** regions separated by a lateral **drift region**. Each **region** is of a different conductivity type.

The lateral **drift region** has a linear lateral doping profile. A conductive field plate is deposited on a linearly-graded **top oxide insulating layer**, increasing from the first to the second region.

USE/ADVANTAGE - For diode or MOSFET. Reduces conduction losses without reducing **breakdown voltage**.

Dwg.1/2

Abstract (Equivalent): US 5648671 A

A lateral **thin-film Silicon**-On-**Insulator** (SOI) device comprising a **semiconductor substrate**, a **thin buried oxide insulating layer** on said **substrate**, and a lateral **semiconductor** device provided in a **thin semiconductor film** on said **thin buried oxide**, said **thin semiconductor film** comprising a first region of a first conductivity type, a second region of a second conductivity type opposite to that of the first and spaced apart from said first **region** by a lateral **drift region** of said second conductivity type having a substantially linear lateral doping profile, a top oxide insulating **layer** over said **thin semiconductor film** and having a substantially linearly-graded portion over a major portion of said lateral **drift region** which increases in thickness from adjacent said first region to adjacent said second region, and a conductive field plate on at least said linearly-graded portion of said **top oxide insulating layer**.

Dwg.2/2

35/3,AB/20 (Item 18 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010705341
WPI Acc No: 1996-202296/199621
Related WPI Acc No: 1994-103266; 2002-207696; 2002-207697; 2002-207698; 2002-228915; 2002-228916
XRPX Acc No: N96-169744

Transistor mfr. method for bipolar, CMOS and DMOS - by forming MOS transistor gate isolated from channel region and adjusting threshold voltage by putting dopants into the channel region with implant energy enough to penetrate gate to implant into channel region

Patent Assignee: SILICONIX INC (SILI-N)
Inventor: CHEN J W; CORNELL M E; WILLIAMS R K; YILMAX H; CHEN W; YILMAZ H
Number of Countries: 005 Number of Patents: 011
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 708482	A2	19960424	EP 95116353	A	19951017	199621	B
US 5541123	A	19960730	US 92948276	A	19920921	199636	
			US 94226419	A	19940411		
			US 94323950	A	19941017		
			US 95463647	A	19950605		
US 5541125	A	19960730	US 92948276	A	19920921	199636	
			US 94226419	A	19940411		
			US 94323950	A	19941017		
			US 95463165	A	19950605		
US 5547880	A	19960820	US 92948276	A	19920921	199639	
			US 94226419	A	19940411		
			US 94323950	A	19941017		
			US 95464978	A	19950605		
US 5559044	A	19960924	US 92948276	A	19920921	199644	
			US 94226419	A	19940411		
			US 94323950	A	19941017		
JP 8227945	A	19960903	JP 95293438	A	19951017	199645	
US 5583061	A	19961210	US 92948276	A	19920921	199704	
			US 94226419	A	19940411		
			US 94323950	A	19941017		

			US 95464435	A	19950605	
US 5618743	A	19970408	US 92948276	A	19920921	199720
			US 94226419	A	19940411	
			US 94323950	A	19941017	
			US 95463417	A	19950605	
EP 708482	A3	19970326	EP 95116353	A	19951017	199728
US 5643820	A	19970701	US 92948276	A	19920921	199732
			US 94226419	A	19940411	
			US 94323950	A	19941017	
			US 95463403	A	19950605	
			US 96667219	A	19960619	
US 5648281	A	19970715	US 92948276	A	19920921	199734
			US 94226419	A	19940411	
			US 94323950	A	19941017	
			US 95463137	A	19950605	
			US 96647073	A	19960508	

Priority Applications (No Type Date): US 94323950 A 19941017; US 92948276 A 19920921; US 94226419 A 19940411; US 95463647 A 19950605; US 95463165 A 19950605; US 95464978 A 19950605; US 95464435 A 19950605; US 95463417 A 19950605; US 95463403 A 19950605; US 96667219 A 19960619; US 95463137 A 19950605; US 96647073 A 19960508

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 708482	A2	E	70	H01L-021/8249	
Designated States (Regional): DE IT NL					
US 5541123	A		67	H01L-021/265	Cont of application US 92948276
					CIP of application US 94226419
					Div ex application US 94323950
					CIP of patent US 5426328
US 5541125	A		67	H01L-021/265	Cont of application US 92948276
					CIP of application US 94226419
					Div ex application US 94323950
					CIP of patent US 5426328
US 5547880	A		66	H01L-021/04	Cont of application US 92948276
					CIP of application US 94226419
					Div ex application US 94323950
					CIP of patent US 5426328
US 5559044	A		66	H01L-021/265	Cont of application US 92948276
					CIP of application US 94226419
					CIP of patent US 5426328
JP 8227945	A		44	H01L-021/8249	
US 5583061	A		67	H01L-021/265	Cont of application US 92948276
					CIP of application US 94226419
					Div ex application US 94323950
					CIP of patent US 5426328
US 5618743	A		66	H01L-021/265	Cont of application US 92948276
					CIP of application US 94226419
					Div ex application US 94323950
					CIP of patent US 5426328
					Div ex patent US 5559044
EP 708482	A3			H01L-021/8249	
US 5643820	A		67	H01L-021/70	Cont of application US 92948276
					CIP of application US 94226419
					Div ex application US 94323950
					Cont of application US 95463403
					CIP of patent US 5426328
					Div ex patent US 5559044
US 5648281	A		69	H01L-021/265	Cont of application US 92948276
					CIP of application US 94226419

Div ex application US 94323950
Cont of application US 95463137
CIP of patent US 5426328
Div ex patent US 5559044

Abstract (Basic): EP 708482 A

The method involves forming a MOS transistor gate (351) overlying and isolated (357) from a channel region (360) on an N-type **substrate** (42). A P-type **source region** (352) is formed. The transistor threshold voltage is adjusted by implanting P+type dopants into the channel region at an implant energy such that the dopants penetrate the gate to implant into the channel region.

The dopants change the threshold voltage. The adjustment is made after forming a diffused **body** (308) or **base region** (310) of another transistor in the same **substrate** to prevent the dopants in the channel region from being subjected to diffusion.

USE/ADVANTAGE - Simultaneously forms bipolar transistors, **high voltage** and low voltage CMOS transistors, DMOS transistors, zener diodes, and **thin film** resistors or any desired combination on same integrated circuit chip.

29a,b,c/35

Abstract (Equivalent): US 5648281 A

A method for forming an isolation structure and a bipolar transistor on a **substrate** layer, said **substrate** layer being of a **semiconductor** material of a first conductivity type, comprising the steps of:

doping a first area on an upper **surface** of said **substrate** layer with dopants of a second conductivity type opposite said first conductivity type to form a first buried region;

doping a second area of said upper **surface** of said **substrate** layer with dopants of said first conductivity type to form a second buried region, said second area being smaller than said first area, said second area being contained within said first area;

forming an epitaxial **layer** over said **upper surface** of said **substrate** layer, said epitaxial layer being of a **semiconductor** material of said second conductivity type, said epitaxial **layer** having an **upper surface**;

extending a well region of said first conductivity type into said epitaxial **layer** from said **upper surface** of said epitaxial layer, said well region being disposed at least partly over said second area, said well region having a bottom **surface** which contacts said second buried region, said second buried region being formed by said dopants of said first conductivity type which doped said second area;

forming a first contact region of said second conductivity type, more highly doped than said epitaxial **layer**, extending from said **upper surface** of said epitaxial layer and contacting said first buried region, wherein said first contact region surrounds said well region;

implanting ions of said second conductivity type into a **base** region of said well region at a first energy and first dosage to form a **base** region of said bipolar transistor;

implanting ions of said second conductivity type into said **base** region at a second energy, less than said first energy, and with a second dosage, greater than said first dosage, to provide a low resistivity **surface** doping of said **base** region of said bipolar transistor; and

implanting ions of said second conductivity type into said **base** region at a third dosage greater than said second dosage to create a **base** contact region at a top **surface** of said

base region of said bipolar transistor to enable ohmic contact between a metal layer contacting said **base** contact region and said **base** region of said bipolar transistor.

Dwg.28/35US 5643820 A

A method for fabricating an MOS capacitor, said process comprising the steps of:

implanting ions of a first conductivity type into an upper **surface** of an epitaxial layer of a second conductivity type, prior to any gate **dielectric layer** being formed on said upper **surface**, to form a highly doped first region of said first conductivity type, said first region being implanted with ions of said first conductivity type with a dose of approximately 1E15 cm2 or greater, said step of implanting also forming a separate zener diode region in said epitaxial layer;

forming a gate **dielectric layer** overlying said first region and overlying one or more channel regions for MOS transistors to be formed; and

forming a conductive **polysilicon layer** overlying said gate **dielectric layer** and overlying said first region and said channel regions such that said conductive **polysilicon layer** is separated from said first region and said channel regions by said gate **dielectric layer**, wherein said first region and said conductive **polysilicon layer** form two plates of said MOS capacitor.

Dwg.31/35

US 5618743 A

A method for forming an MOS transistor in conjunction with transistors of a different type in the same **substrate** comprising the steps of:

forming a gate of said MOS transistor overlying and isolated from a channel region of a **semiconductor** material of a first conductivity type;

forming a **source region** of a second conductivity type lowering a threshold voltage of said MOS transistor by implanting dopants of said second conductivity type into said channel region in said **semiconductor** material at an implant energy such that said dopants of said second conductivity type penetrate said gate to implant into said channel region underlying said gate, said dopants being sufficient to lower a threshold voltage of said MOS transistor to achieve a desired threshold so that said MOS transistor is capable of being selectively controlled to change between a conductive state and a nonconductive state,

said step of lowering a threshold voltage of said MOS transistor occurring after a diffusion step for forming a diffused **body** or **base region** of another transistor in said same **substrate** to prevent said dopants of said second conductivity in said channel region from being subjected to said diffusion step,

wherein said step of forming said **source region** comprises patterning a photoresist masking layer overlying said **semiconductor** material and depositing dopants of said second conductivity type into exposed portions of said **semiconductor** material, and wherein said step of lowering a threshold voltage is conducted while said photoresist masking layer remains overlying said **semiconductor** material so that said step of lowering said threshold voltage does not require another masking step.

29b,c/35

US 5583061 A

A method for forming at least two PMOS transistors having different intended **breakdown voltages**, said method comprising the steps of:

forming a first gate of a first PMOS transistor, said first gate having a length of approximately 2 microns to achieve a first **breakdown voltage;**

forming a second gate of a second PMOS transistor, said second gate having a length of approximately 2.5 microns to achieve a higher **breakdown voltage** than said first **breakdown voltage;**

implanting P-type dopants at a first energy and a first dosage using a first mask to form **source** and drain **regions** for said first PMOS transistor and said second PMOS transistor, said first energy being insufficient to cause said dopants to penetrate through said gate, said **source** and drain **regions** being self-aligned with said first gate and said second gate; and

implanting P-type dopants through said first gate and said second gate at a second energy higher than said first energy and a second dosage lower than said first dosage to adjust a threshold voltage of said first PMOS transistor and said second PMOS transistor such that said first PMOS transistor and said second PMOS transistor are formed using the same process steps, said step of implanting P-type dopants through said first gate and said second gate being conducted using said first mask.

29A,29C/35

US 5559044 A

A method for forming a DMOS transistor and a bipolar transistor in a same **substrate** comprising the steps of:

forming a gate of said DMOS transistor overlying said **substrate;**

implanting ions of a first conductivity type into a first region of a **semiconductor** material of a second conductivity type at a first energy and dosage;

driving in said ions of said first conductivity type to form a body of said DMOS transistor, said body being formed so as to cause said DMOS transistor to have desired operating characteristics;

implanting said ions of said first conductivity type into a second region of said **semiconductor** material at a second energy and second dosage, said second energy being less than said first energy, said step of implanting said ions into said second region being conducted after the formation of said body of said DMOS transistor;

driving in said ions of said first conductivity type in said second region to form a **base** region of said bipolar transistor, said **base** region being shallower and more highly doped than said body to provide said bipolar transistor with desired operating characteristics;

implanting ions of said first conductivity type into said second region at a third energy, less than said second energy, and with a third dosage, greater than said second dosage, to provide a low resistivity **surface** doping of said **base** region of said bipolar transistor; and

implanting ions of said first conductivity type into said second region at a fourth dosage greater than said third dosage to create a **base** contact region at a top **surface** of said **base** region of said bipolar transistor to enable ohmic contact between a metal layer contacting said **base** contact region and said **base** region of said bipolar transistor.

Dwg.27/35

US 5547880 A

A method for forming a zener diode region and an isolation region comprising the steps of:

forming an isolation region of a first conductivity type extending from a first **surface** area of an epitaxial layer of a second

conductivity type and contacting a **semiconductor** material of said first conductivity type located below said first **surface** area, said isolation region having a first impurity concentration; and

implanting ions of said first conductivity type into a second **surface** area of said epitaxial layer, after said step of forming an isolation region, to form a zener diode region of said first conductivity type in said second **surface** area for use in forming a zener diode having a selected reverse **breakdown voltage**, said zener diode region having a second impurity concentration higher than said first impurity concentration,

said step of implanting also including implanting said ions in said first **surface** area to additionally dope said isolation region.

Dwg.31/35

US 5541125 A

A method for forming a lateral MOS transistor having a lightly doped drain for increased **breakdown voltage** and for forming other transistors in the same **substrate**, said method comprising the steps offorming a first gate for a lateral MOS transistor and a second gate for a DMOS transistor overlying and insulated from a **semiconductor** material;

forming a first masking layer over said **semiconductor** material to mask a first area around said first gate and expose a second area around said second gate;

implanting ions of a first conductivity type into said second area using said second gate and said first masking layer as a mask for forming a self-aligned **body region** of said first conductivity type for said DMOS transistor;

removing said first masking layer to expose said first area around said first gate and expose said second area around said second gate;

implanting ions of a second conductivity type into said first area and said second area, said first gate and said second gate acting as a mask to self-align implantation of said ions of said second conductivity type with said first gate and said second gate, said ions of said second conductivity type counter-doping said **body region** of said DMOS transistor and forming a lightly doped drain of said lateral transistor self-aligned with said first gate,

said step of implanting said ions of said first conductivity type being adjusted to take into account said counter-doping from said implantation of said ions of said second conductivity type into said **body region** so that said **body region** has desired electrical characteristics;

forming a second masking layer over a portion of said lightly doped drain to leave an exposed portion of said lightly doped drain; and

implanting ions of said second conductivity type into said **body region** to form a **source region** of said DMOS transistor and into said exposed portion of said lightly doped drain to form a drain region of said lateral MOS transistor spaced from said first gate.

Dwg.15a/35

US 5541123 A A method for forming a bipolar transistor to achieve a selected **breakdown voltage** comprising the steps of:

forming a **base** region of a first conductivity type in a **semiconductor** material of a second conductivity type;

forming a collector contact region of a second conductivity type in said **semiconductor** material of said second conductivity type;

forming a **base** contact region of said first conductivity type in said **base** region, said **base** contact region being more highly doped than said **base** region, said **base** contact region being spaced from a closest edge of said **base** region so as to increase a distance between said **base** contact region and said

collector contact region, said distance being sufficient to avoid breakdown between said **base** contact region and said collector contact region through said **semiconductor** material of said second conductivity type; and

forming a first region of said second conductivity type, but more lightly doped than said collector contact region, between said collector contact region and said **base** region to increase a **breakdown voltage** between said **base** contact region and said collector contact region,

wherein said collector contact region and said first region surround said **base** region at a **surface** of said **semiconductor** material.

Dwg.33/35

35/3,AB/21 (Item 19 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010007010
WPI Acc No: 1994-274721/199434
XRPX Acc No: N94-216622
Metal oxide **semiconductor** field effect transistor - has low impurity concentration slits formed between drift and diffusion layers
Patent Assignee: SHARP KK (SHAF)
Inventor: KARIYAMA M
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 6204476	A	19940722	JP 93452	A	19930106	199434	B
US 5510643	A	19960423	US 93149109	A	19931109	199622	
JP 2997377	B2	20000111	JP 93452	A	19930106	200007	

Priority Applications (No Type Date): JP 93452 A 19930106
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 6204476	A		6	H01L-029/784	
JP 2997377	B2		7	H01L-029/78	Previous Publ. patent JP 6204476
US 5510643	A		10	H01L-027/092	

Abstract (Basic): JP 6204476 A

The MOSFET includes a p=type **semiconductor substrate** (1) in which n=type diffusion layer (35) is formed. The p=type drift layer (12) is formed with the p=type source diffusion layer (15) on one side and with a drain diffusion layer (16) on the other side. A **silicon oxide film** (17) is formed over the top **surface** using chemical vapour deposition techniques.

A source electrode (18) and drain electrode (19) are formed in the **silicon oxide film** openings. The n=type diffusion layer is formed with lowered impurity concentration near the drift layer. This low concentration impurity domain is demarcated as slits (20,21).

ADVANTAGE - Eases electric field generator between diffusion and drift layers. Raises reverse pressure proof characteristics. Controls punch phenomenon between **source** and drain **regions**. Facilitates magnetisation of gate electrodes and this in turn minimises structure of whole **semiconductor** device.

Dwg.1/7

Abstract (Equivalent): US 5510643 A

A **semiconductor** device including a **high voltage** MOS transistor comprising:

a first conductivity type **semiconductor substrate** having an upper **surface**;

a second conductivity type tub formed in the first conductivity type **semiconductor substrate**, said tub extending to said upper **surface**, said tub including a portion at an upper **surface** of said tub, said portion having a second conductivity impurity concentration;

at least one predetermined slit region formed within and surrounded laterally by said portion, said at least one predetermined slit region having a lower second conductivity type impurity concentration than the second conductivity type impurity concentration of said portion;

first conductivity type **source**/drain **regions** within and surrounded by said portion formed in said tub and extending from said upper **surface**; and

at least one of said first conductivity type **source**/drain **regions** having a first conductivity type drift layer connected thereto, said first conductivity type drift layer extending toward the other of said first conductivity type **source**/drain **regions**;

wherein said at least one predetermined slit region contacts at least said drift layer from said portion to thereby increase the reverse **breakdown voltage** of said transistor.

Dwg.3e,7

35/3,AB/22 (Item 20 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009133434
WPI Acc No: 1992-260872/199232
Related WPI Acc No: 1993-207189; 1994-357466
XRAM Acc No: C92-116497
XRPX Acc No: N92-199476

Mfr. of integrated circuit devices by **semiconductor**-on-insulator technology - for **high voltage** application improving voltage breakdown

Patent Assignee: PHILIPS ELECTRONICS NV (PHIG); PHILIPS GLOEILAMPENFAB NV (PHIG); NORTH AMERICAN PHILIPS CORP (PHIG); US PHILIPS CORP (PHIG)
Inventor: ARNOLD E; MERCHANT S; MERCHANT S L
Number of Countries: 007 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 497427	A2	19920805	EP 92200252	A	19920129	199232	B
JP 4309234	A	19921030	JP 9215324	A	19920130	199250	
EP 497427	A3	19930310	EP 92200252	A	19920129	199349	
US 5300448	A	19940405	US 91650391	A	19910201	199413	
			US 9315061	A	19930208		
EP 497427	B1	19960410	EP 92200252	A	19920129	199619	
DE 69209678	E	19960515	DE 609678	A	19920129	199625	
			EP 92200252	A	19920129		
US 5767547	A	19980616	US 91650391	A	19910201	199831	
			US 9315061	A	19930208		
			US 93165602	A	19931209		
			US 95448268	A	19950523		

Priority Applications (No Type Date): US 91650391 A 19910201; US 9315061 A 19930208; US 93165602 A 19931209; US 95448268 A 19950523
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes

EP 497427 A2 E 11 H01L-029/784
Designated States (Regional): DE FR GB IT NL
JP 4309234 A 8 H01L-021/336
US 5300448 A 11 H01L-021/266 Cont of application US 91650391
EP 497427 B1 E 13 H01L-029/772
Designated States (Regional): DE FR GB IT NL
DE 69209678 E H01L-029/772 Based on patent EP 497427
US 5767547 A H01L-027/01 Cont of application US 91650391
Div ex application US 9315061
Cont of application US 93165602
Div ex patent US 5300448
EP 497427 A3 H01L-029/784

Abstract (Basic): EP 497427 A

A method of mfg. a **high voltage** thin **film** transistor in a **thin layer** of monocrystalline **silicon** provided over an **oxide layer** on **silicon substrate,** comprises: forming a mask with numerous openings of progressively increasing dimensions over the **thin layer** of **silicon** and introducing impurities into the silicon through the openings forming numerous doped regions of different width. The mask is then removed and the layer is annealed to form a nearly linear doping profile over the silicon. A transistor structure is formed with the **silicon layer** having a linear doping profile.

A **high voltage thin film silicon**-on-**insulator** transistor is claimed comprising: a **thin layer** of monocrystalline **silicon** of first conductivity having a linear doping profile from one side to the other, and the **thin** layer on a **buried oxide layer** on a silicon **substrate,** an oxide **layer** over the **thin layer,** a **polysilicon** gate region in contact with the second conductivity portion, a **source region** adjacent to gate region, a drain region in contact with first conductivity type, and electrodes disposed through **oxide layer** contacting the **source**, gate and drain **regions.**

USE/ADVANTAGE - Integrated circuit devices manufactured by **semiconductor**-on-insulator technology exhibiting improved voltage breakdown, esp. for very thin (less than 1 micron) films.

Dwg.11/16

Abstract (Equivalent): EP 497427 B

A **high voltage thin film** transistor of an SOI type comprising (a) a **thin layer** (1) of **silicon** comprising a region (5) of a first conductivity type, said **thin layer** being disposed on a **buried layer** (2) of an **oxide,** said thin **layer** and said **buried layer** being disposed on a silicon **substrate** (3), (b) a **layer** of an **oxide** disposed over said **thin layer;** (c) a **polysilicon** gate region (7) disposed in contact with a portion (9) of a second conductivity type within said layer at one side of said **region** (5), (d) a **source region** (11) within said **thin layer** disposed adjacent said gate region at a side opposite to said region (5) of said **thin layer** of said first conductivity type, (e) a drain region disposed at said second opposite end of said region (5) of said first conductivity type, and (f) electrodes disposed through said **layer** of **oxide** to respectively contact said **source region,** said gate **region,** and said drain region, characterised in that said region (5) of said first conductivity type has a linear doping profile from its one side to a second opposite side, and in that said **thin layer** (1) is comprised of monocrystalline silicon.

Dwg.1A/6

Abstract (Equivalent): US 5300448 A

High voltage TFT(s) are mfd. by (a) forming a **thin layer** of monocrystalline **Si** over an **oxide layer** on an **Si substrate,** (b) decreasing the resistivity of the **Si layer** by uniformly introducing impurities, (c) forming a mask over the **Si layer,** each opening in the mask laterally increasing in dimension from that of a preceeding opening, (d) introducing impurities through the openings to form doped regions at different width, (e) removing the mask, capping with an Si3N4 layer and annealing to form a linear doping profile over a lateral distance, (f) removing the Si3N4 at regions beyond edges of the lateral distance, thermally oxidising exposed Si areas and then removing remaining portions of Si3N4, and (g) forming a structure with the **Si thin layer**. The linear doping profile is formed with a min. doping concn. at one end of the lateral distance and a max. doping concn. at the opposite end.

The annealing is carried out fro 18-36 hours, at 1150 deg. C.

ADVANTAGE - Significantly increased **breakdown voltage,** esp. for very **thin** (below (micron)) SOI **films.**

Dwg.2f/6

35/3,AB/23 (Item 21 from file: 350)

DIALOG(R)File 350:Derwent WPIX

004666595

WPI Acc No: 1986-169937/198627

XRAM Acc No: C86-072987

XRPX Acc No: N86-126815

High **breakdown voltage** MOS transistor prodn. - in fully dielectrically insulated **substrate**

Patent Assignee: TECH HOCH LLMENAU (TEHO-N)

Inventor: DJERMANOV I; SCHIPANSK D; SCHMIDT J

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DD 233688	A	19860305	DD 272122	A	19841229	198627	B

Priority Applications (No Type Date): DD 272122 A 19841229

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DD 233688	A		7		

Abstract (Basic): DD 233688 A

A MOS **high voltage** transistor is produced in completely dielectrically insulated **substrates** by (i) producing field oxide regions by selective oxidn. over an n-conducting Si ditch; (ii) growing a 80-100 nm. thick gate **oxide layer;** (iii) depositing and structuring a poly **Si layer;** (iv) implanting acceptor ions (e.g. B ions) through a lacquer mask only into the **source region** of the DMOS transistor; (v) removing the lacquer layer; (vii) deeply diffusing the channel region; and (viii) high dosage implanting donor ions (e.g. P ions), followed by tempering at 1100-1200 deg. C.

The novelty is that (a) completely dielectrically insulated **substrates** are used as starting material; (b) the poly **Si layer** is structured so that it forms a field plateau over the drift zone of the transistor; (c) the low ditch depth of the

substrate material results in an almost planar pn-junction between the **drift** and channel **regions**; and (d) additional **source** and drain field plateaus are provided to obtain high **breakdown voltages**.

ADVANTAGE - DMOS transistors having **breakdown voltages** of about 400 V are produced rapidly and without insulation problems in fully dielectrically insulated **substrates**. (7pp Dwg.No.0/10)

35/3,AB/24 (Item 22 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004503627
WPI Acc No: 1986-006971/198601
XRPX Acc No: N86-005062
Tri-well CMOS structure with three or more active regions - has thick oxide formed at inter-well boundaries so that edges of three wells are automatically self-aligned
Patent Assignee: AMER MICROSYSTEMS I (AMMI-N); JOY R C (JOYR-I)
Inventor: BATRA T L
Number of Countries: 008 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 8505736	A	19851219	WO 85US990	A	19850522	198601	B
EP 182876	A	19860604	EP 85902890	A	19850522	198623	
JP 61502993	W	19861218	JP 85502457	A	19850522	198705	
CA 1239707	A	19880726				198833	
EP 182876	B	19901024				199043	
DE 3580247	G	19901129				199049	

Priority Applications (No Type Date): US 84614418 A 19840525
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
WO 8505736 A E 33
Designated States (National): JP
Designated States (Regional): DE FR GB IT NL SE
EP 182876 A E
Designated States (Regional): DE FR GB NL SE
EP 182876 B
Designated States (Regional): DE FR GB IT SE

Abstract (Basic): WO 8505736 A

The **semiconductor substrate** (60) includes a moderately to heavily doped well (71) of the same conductivity type as the **substrate**. A second moderately-to-heavily-doped well (65) of the opposite conduct conductivity type to the **substrate** is formed. A third lightly doped region (68) of either type is formed of the same order of conductivity as the **substrate**.

Thick oxide is formed at inter-well boundaries to prevent parasitic current paths forming between devices. Gates (121,123), for the active devices in the wells are formed next. **Source** and drain **regions** are provided (145,146,147) in each of the N well, P well and **high voltage** regions.

ADVANTAGE - The number of mesking steps required is less, so increasing yield, at lower cost
Abstract (Equivalent): EP 182876 B

A method of forming wells (65,68,71) in a semi-conductor **substrate** (60) comprising: depositing a **thin layer** of **oxide** (61) on said **substrate** (60), deposition a **layer**

of **silicon** nitride (62) on said **thin layer** of **oxide** (61), initiating a process to be repeated at least two times of: applying a layer of photoresist (63), removing portions (64) of said photoresist (63), thereby exposing portions of said silicon nitride (62), removing exposed portions of said silicon nitride (62) and thin oxide (61), thus creating exposed portions of said **semiconductor substrate** (60), implanting dopants of a selected conductivity type to a selected concentration into said exposed portions of said **semiconductor substrate** (60), thereby forming a well (65) of said selected conductivity type having a **breakdown voltage** determined by said selected concentration, and oxidising said exposed portions of said **semiconductor substrate** (60) thus creating protective thick oxide (66) over said exposed portions and diffusing said dopants into said **semiconductor substrate** (60), said thick oxide (66) serving as a mask during subsequent repetitions of said process and causing subsequent wells (68), to be self aligned with wells (65,68) beneath said thick oxide (66,69), and after sufficient repetition of said process moving said protective thick oxide (66,69). (14pp)

35/3,AB/25 (Item 23 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003992642
WPI Acc No: 1984-138185/198422
XRAM Acc No: C84-058569
XRPX Acc No: N84-102344
MIS-type **semiconductor** devices - with depletion zone in gate electrode adjacent to dielectric
Patent Assignee: PHILIPS GLOEILAMPENFAB NV (PHIG)
Number of Countries: 007 Number of Patents: 011
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
NL 8203870	A	19840501	NL 823870	A	19821006	198422	B
EP 111347	A	19840620	EP 83201409	A	19831003	198425	
JP 59087869	A	19840521	JP 83186077	A	19831006	198426	
US 4586064	A	19860429	US 83539446	A	19831006	198620	
US 4590506	A	19860520	US 83539447	A	19831006	198623	
US 4590509	A	19860520	US 83539448	A	19831006	198623	
EP 111347	B	19870311				198710	
DE 3370249	G	19870416				198716	
JP 1046980	A	19890221	JP 88184769	A	19880000	198913	
JP 1046981	A	19890221	JP 88184770	A	19880000	198913	
JP 92058700	B	19920918	JP 83186077	A	19831006	199242	

Priority Applications (No Type Date): NL 823870 A 19821006; EP 83201409 A 19831003
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
NL 8203870	A		39		
EP 111347	A	E			
Designated States (Regional): DE FR GB IT					
EP 111347	B	E			
Designated States (Regional): DE FR GB IT					
JP 92058700	B		10	H01L-027/148	Based on patent JP 59087869

Abstract (Basic): EP 111347 A
A **semiconductor** device comprising an element of the MIS type

having a monocrystalline **semiconductor** body, one **surface** of which is provided with a comparatively **thin dielectric layer** which constitutes a gate dielectric of the MIS element and on which is formed a gate electrode of doped **semiconductor** material of mainly one conductivity type for influencing the **surface** potential in the **semiconductor** body, the doped **semiconductor** material having to be used otherwise than as resistor, and being provided with an ohmic connection for supplying gate voltages, characterised in that at least a part referred to hereinafter as a high-ohmic part of the gate electrode adjoining the gate dielectric has such a low doping concentration and such a conductivity type that under usual operation conditions, whilst avoiding breakdown, a depletion layer can be formed, which extends from the gate dielectric into the high-ohmic part of the gate electrode, as a result of which a decoupling between the **semiconductor** body and the gate electrode can be obtd. temporarily and/or locally. (23pp)

Abstract (Equivalent): EP 111347 B

A **semiconductor** device comprising an element of the MIS type having a monocrystalline **semiconductor** body, one **surface** of which is provided with a comparatively **thin dielectric layer** which constitutes a gate dielectric of the MIS element and on which is formed a gate electrode of doped **semiconductor** material of mainly one conductivity type for influencing the **surface** potential in the **semiconductor** body, the doped **semiconductor** material having to be used otherwise than as resistor, and being provided with an ohmic connection for supplying gate voltages, characterised in that at least a part referred to hereinafter as a high-ohmic part of the gate electrode adjoining the gate dielectric has such a low doping concentration and such a conductivity type that under usual operation conditions, whilst avoiding breakdown, a depletion layer can be formed, which extends from the gate dielectric into the high-ohmic part of the gate electrode, as a result of which a decoupling between the **semiconductor** body and the gate electrode can be obtd. temporarily and/or locally.

Abstract (Equivalent): US 4590509 A

A **semiconductor** device with an MIS type element has a monocrystalline body with a **thin dielectric layer** on one **surface** forming the element gate dielectric and on which is a doped **semiconductor** gate electrode for influencing body **surface** potential and which is electrically decoupled from the body by a high-resistivity part of the electrode adjoining the dielectric.

The part has low dopant concn. and conductivity type such that while avoidingbreakdown a depletion layer can be formed extending from the dielectric into the high-resistivity part. The device has a **high-voltage** element and the high-resistivity part comprises a field plate with adjacent regions of opposite conductivity type to form a rectifying junction for draining minority charge carriers. The **high-voltage** element is pref. an insulated gate FET.

ADVANTAGE - Provides a controllable quasi-thickened part of the dielectric.

(17pp)

US 4590506 A

A charge-coupled buried channel **semiconductor** device having an MIS element has the element gate **dielectric** as a **thin layer** on a monocrystalline **semiconductor** body, with a doped **semiconductor** gate electrode on the layer for influencing body **surface** potential and electrically decoupled from the body by a high-resistivity part of the electrode adjoining the dielectric with

low dopant concn. and conductivity type such as to form a depletion layer extending from the layer into the part.

Spaced gate electrodes and a subadjacent channel form a row of clock electrodes as a continuous **layer** of polycrystalline **Si** devided into high-resistivity parts separated by electrically floating parts. The high-resistivity parts are of diff. conductivity type to the channel **surface** which is no more than 1.0 microns thick and isolated on its other side by a p-n junction.

ADVANTAGE - Provides favourable potential distribution in the **substrate**.

(16pp)

US 4586064 A

Semiconductor device comprises a MIS element with a mono-crystalline **semiconductor** body on the **surface** of which is a **thin dielectric layer** which forms the gate dielectric of the MIS element.

A gate electrode of doped **semiconductor** material is formed on this layer, and a high resistivity part of the gate electrode (50) adjoining the gate dielectric electrically decouples the gate electrode (50) from the **semiconductor** body. A depletion layer (52) is formed which extends from the gate dielectric into the high resistivity part of the electrode.

The **semiconductor** element is a double diffused IGFET in which the **source** zone and channel **region** are formed **surface** zones of opposite conductivity, the second zone at least partly surrounding the first zone.

An intermediate high resistance **drift region** (42) separates the second zone from the drain zone of the first zone.

The gate electrode comprises a weakly doped part of the same conductivity as the second zone which is above the drift zone, and is connected to the transistor drain (44) through a rectifying pn junction (53).

USE/ADVANTAGE - CCD or D-MOST mfr.

Parasitic capacities are reduced and the **breakdown voltage** at the edge of the field plate is increased.

(16pp

35/3,AB/26 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06691895
SEMICONDUCTOR DEVICE

PUB. NO.: 2000-277725 [JP 2000277725 A]
PUBLISHED: October 06, 2000 (20001006)
INVENTOR(s): GOSHIMA SUMITAKA
APPLICANT(s): SEIKO INSTRUMENTS INC
APPL. NO.: 11-084290 [JP 9984290]
FILED: March 26, 1999 (19990326)

ABSTRACT

PROBLEM TO BE SOLVED: To increase the reverse **breakdown voltage** of a PN junction of a **high voltage** insulated-gate field-effect transistor by forming a low-concentration drain region of low impurity and a first conductivity low-concentration isolation region of low impurity, isolating them from each other.

SOLUTION: On the **surface** of a P-type silicon **substrate** 1, an

N+-type **source region** 2 and an N+-type drain region 3 are formed. Between the **source region** 2 and the drain region 3, a channel region 7 is formed. On the channel region 7, a gate electrode 9 of a polycrystalline **silicon film** is formed with a gate **insulating film** 8 of a **silicon oxide film** in between. Between the drain region 3 and the channel region 7, a low-concentration N+--type drain region 4 of low concentration is caused to exist. Besides, a field **insulating film** 5 is formed on the low-concentration drain region 4. To increase the **breakdown voltage** between the drain region 3 and the silicon **substrate** 1, an N--type WELL region 6 is formed in the periphery of the drain region 3.

35/3,AB/27 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06505880
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 2000-091597 [JP 2000091597 A]
PUBLISHED: March 31, 2000 (20000331)
INVENTOR(s): TOMII KAZUYUKI
SUGIURA YOSHIYUKI
APPLICANT(s): MATSUSHITA ELECTRIC WORKS LTD
APPL. NO.: 10-258870 [JP 98258870]
FILED: September 11, 1998 (19980911)

ABSTRACT
PROBLEM TO BE SOLVED: To make it possible to suppress reduction in an anode-cathode **breakdown voltage** even in the case where a **high potential** wiring is performed from the side of a cathode to the side of an anode astride the upper part of a **drift region**.

SOLUTION: A p+ anode region 2, which is a heavily doped second conductivity type region, and an n+ cathode region 3, which is a heavily doped first conductivity type region, are formed holding a **drift region** between them in the main **surface** on one side of the main **surfaces** of an N-type **semiconductor substrate** 1 which is a lightly doped first conductivity type. Moreover, an **insulating layer** 4, such as a **silicon oxide film**, is formed on the main **surface** on one side of the main **surfaces** of the **substrate** 1 and field plates 5a and 5b are respectively connected electrically with the regions 2 and 3 for making an electric field in the **surfaces** of the regions 2 and 3 relax. A **high potential** wiring 6 is electrically connected with the region 3 astride the upper part of the **drift region** . An electrically insulated floating conductor 7 is provided within the layer 4 on the **drift region**.

35/3,AB/28 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

04335270

NONVOLATILE **SEMICONDUCTOR** MEMORY

PUB. NO.: 05-326970 [JP 5326970 A]
PUBLISHED: December 10, 1993 (19931210)
INVENTOR(s): SUMIHIRO NAOTAKA
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-080172 [JP 9280172]
FILED: April 02, 1992 (19920402)
JOURNAL: Section: E, Section No. 1521, Vol. 18, No. 144, Pg. 63, March 10, 1994 (19940310)

ABSTRACT

PURPOSE: To prevent a depletion in the proximity of the drain **surface** under a tunnel **oxide film** and reduce a memory cell size, by stacking a low conectration N-type **semiconductor** layer and a high concentration N-type **semiconductor** layer and installing **source** and drain **regions** in a protrusion shape so as to connect their regions to a P-type **semiconductor substrate** only the bottom of the low concentration N-type **semiconductor** layer.

CONSTITUTION: A **source region** 2 and a drain region 3 of a MOS transistor for memory and a **source region** 4 and a drain region 5 of a MOS transistor for selection have a stacked structure of a low concentration N-type **semiconductor** layer 6 and a high concentration N-type **semiconductor** layer 7. Further, their regions are installed on a P-type silicon **substrate** 1 in a protrusion shape so as to have the connecting **surface** to the P-type silicon **substrate** 1 only on the bottom of the N-type **silicon semiconductor layer** 6. Thus, when applying a **high voltage**, a depletion layer spreads only from the bottom of the drain region and does not spread from a channel region transversely. Also, an avalanche **breakdown voltage** does not affect a channel length. Accordingly, a memory cell size can be reduced.

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 04may04 14:19:00 User267149 Session D1372.1

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  File 350:Derwent WPIX 1963-2004/UD,UM &UP=200427
         (c) 2004  Thomson Derwent
*File 350: For more current information, include File 331 in your search.
Enter HELP NEWS 331 for details.
  File 347:JAPIO Nov 1976-2003/Dec(Updated 040402)
         (c) 2004 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.
  File 344:Chinese Patents Abs Aug 1985-2004/Mar
         (c) 2004 European Patent Office
  File 371:French Patents 1961-2002/BOPI 200209
         (c) 2002 INPI.  All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.
```

Set	Items	Description
S1	97	AU=(LETAVIC, T? OR LETAVIC T?)
S2	2526	AU=(SIMPSON, M? OR SIMPSON M?)
S3	36	S1 AND S2
S4	24	S3 AND SEMICONDUCT?
S5	21	S4 AND HIGH????()(VOLT? OR POTENTIAL?)
S6	17	RD (unique items)
S7	13	S6 AND (SILICON OR SI)(3N)(LAYER??? OR FILM??? OR COAT??? - OR MULTILAYER??? OR MULTI()LAYER????? OR SPACER??? OR INTERLA-YER???? OR INTER()LAYER????? OR MULTIPLE()LAYER? ?)
S8	4	S6 NOT S7

7/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7412062 INSPEC Abstract Number: B2002-11-2560P-015
Title: Thin-**layer** **silicon**-on-insulator **high-voltage** PMOS device and application
Author(s): **Letavic, T.**; Albu, R.; Dufort, B.; Petruzzello, J.; **Simpson, M.**; Mukherjee, S.; Weijland, I.; van Zwol, H.
Author Affiliation: Philips Res. USA, Briarcliff Manor, NY, USA
Conference Title: Proceedings of the 14th International Symposium on Power Semiconductor Devices and ICs (Cat. No.02CH37306) p.73-6
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA xx+311 pp.
ISBN: 0 7803 7318 9 Material Identity Number: XX-2002-01938
U.S. Copyright Clearance Center Code: 0-7803-7318-9/02/$17.00
Conference Title: Proceedings of the 14th International Symposium on Power Semiconductor Devices and ICs
Conference Sponsor: IEEE Electron Devices Soc.; Inst. Electr. Eng. Japan
Conference Date: 4-7 June 2002 Conference Location: Sante Fe, NM, USA
Language: English
Abstract: We present a thin-**layer silicon**-on-insulator (SOI) **high-voltage** PMOS device structure and measured performance characteristics. The all-implanted device structure supports voltage by multi-dimensional depletion from a combination of implanted surface pn junctions and MOS capacitor structures formed with multi-level dielectric deposition and metallization. A graded-doped body region has been optimized for application voltages from 100-600 V, and the structure has been evaluated in applications including **high-voltage** level shifting, low-dissipation bias networks, and **high-voltage** high-frequency class AB power output stages. The integrated **high-voltage** PMOS device structure enables low-power, **high voltage** , and high-speed complementary circuit topologies to be realized in a thin-layer SOI process flow, improving circuit efficiency and expanding the application base for thin-layer technology.
Subfile: B
Copyright 2002, IEE

7/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6475749 INSPEC Abstract Number: B2000-02-1210-052
Title: 600 V power conversion system-on-a-chip based on thin **layer** **silicon**-on-insulator
Author(s): **Letavic, T.**; **Simpson, M.**; Arnold, E.; Peters, E.; Aquino, R.; Curcio, J.; Herko, S.; Mukherjee, S.
Author Affiliation: Philips Res., Philips Electron. North America Corp., Briarcliff Manor, NY, USA
Conference Title: 11th International Symposium on Power Semiconductor Devices and ICs. ISPSD'99 Proceedings (Cat. No.99CH36312) p.325-8
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1999 Country of Publication: USA xxiii+359 pp.
ISBN: 0 7803 5290 4 Material Identity Number: XX-1999-02322
U.S. Copyright Clearance Center Code: 0 7803 5290 4/99/$10.00
Conference Title: 11th International Symposium on Power Semiconductor Devices and ICs. ISPSD '99
Conference Sponsor: IEEE Electron Devices Soc.; Inst. Elec. Eng. of Japan
Conference Date: 26-28 May 1999 Conference Location: Toronto, Ont.,

Canada
Language: English
Abstract: An integrated 600 V power conversion system is described based on smart power technology which combines novel lateral **high-voltage** RESURF transistor structures and a merged bipolar/CMOS/DMOS process flow on thin-layer SOI substrates. A new **high-voltage** SOI LDMOS device structure is presented which results in a factor-of-two decrease in specific on-resistance and a factor-of-two improvement in source-follower saturated current, thus overcoming a key limitation of integrated thin-layer technology. This opens new application areas for thin-layer SOI, such as lighting electronics, power modules, motor control, and others, a significant development for the integration of power conversion systems.
Subfile: B

7/3,AB/3 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05930449
E.I. No: EIP01446710200
Title: Lateral smart-discrete process and devices based on thin-**layer silicon**-on-insulator
Author: **Letavic, T.**; Petruzzello, J.; **Simpson, M.**; Curcio, J. ; Mukherjee, S.; Davidson, J.; Peake, S.; Rogers, C.; Rutter, P.; Warwick, M.; Grover, R.
Corporate Source: Philips Research USA, Briarcliff Manor, NY 10510, United States
Conference Title: 13th International Symposium on Power Semiconductor Devices and ICs (ISPSD'01)
Conference Location: Osaka, Japan Conference Date: 20010604-20010607
E.I. Conference No.: 58615
Source: IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD) 2001. p 407-410 (IEEE cat n 01CH37216)
Publication Year: 2001
CODEN: PISDEK
Language: English
Abstract: A ten-mask lateral smart-discrete process technology which combines novel **high-voltage** RESURF transistor structures and a merged bipolar/DMOS process flow on thin-layer SOI substrates is presented. Benchmarking shows that 650V/1.2 Ohm SOI lateral smart-discrete devices exhibit a total gate charge which is a factor-of-two lower than vertical super junction devices, a temperature-independent body diode reverse recovery time which is a factor-of-two smaller than vertical ultra-fast silicon diodes, and total hard-switching losses which are lower than conventional VDMOS. The total gate charge, reverse recovery time, and switching delay times are the lowest reported values for 650V silicon devices. This, in conjunction with a process with integrated logic, establishes SOI smart-discrete technology as best-in-class for efficient high-frequency power conversion. 8 Refs.

7/3,AB/4 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05413027
E.I. No: EIP99114893857

Title: 600V power conversion system-on-a-chip based on thin **layer silicon**-on-insulator
Author: **Letavic, T.**; **Simpson, M.**; Arnold, E.; Peters, E.; Aquino, R.; Curcio, J.; Herko, S.; Mukherjee, S.
Corporate Source: Philips Electronics North America Corp, Briarcliff Manor, NY, USA
Conference Title: Proceedings of the 1999 11th International Symposium on Power Semiconductor Devices and IC's, ISPSD'99
Conference Location: Toronto, Ont, Can Conference Date: 19990526-19990528
E.I. Conference No.: 55507
Source: IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD) 1999. p 325-328
Publication Year: 1999
CODEN: PISDEK
Language: English
Abstract: An integrated 600 V power conversion system is described based on smart power technology which combines novel lateral **high-voltage** RESURF transistor structures and a merged Bipolar/CMOS/DMOS process flow on thin-layer SOI substrates. A new **high-voltage** SOI LDMOS device structure is presented which results in a factor-of-two decrease in specific on-resistance and a factor-of-two improvement in source-follower saturated current, thus overcoming a key limitation of integrated thin-layer technology. This opens new application areas for thin-layer SOI, such as lighting electronics, power modules, motor control, and others, a significant development for the integration of power conversion systems. (Author abstract) 5 Refs.

7/3,AB/5 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04814964
E.I. No: EIP97093816238
Title: High performance 600 V smart power technology based on thin **layer silicon**-on-insulator
Author: **Letavic, T.**; Arnold, E.; **Simpson, M.**; Aquino, R.; Bhimnathwala, H.; Egloff, R.; Emmerik, A.; Wong, S.; Mukherjee, S.
Corporate Source: Philips Electronics North America Corp, Briarcliff Manor, NY, USA
Conference Title: Proceedings of the 1997 9th International Symposium on Power Semiconductor Devices and ICs, ISPSD
Conference Location: Weimer, Ger Conference Date: 19970526-19970529
E.I. Conference No.: 46957
Source: IEEE International Symposium on Power Semiconductor Devices & ICs (ISPSD) 1997. IEEE, Piscataway, NJ, USA,97CH36086. p 49-52
Publication Year: 1997
CODEN: PISDEK
Language: English
Abstract: A high-performance 600 V smart power technology has been developed in which novel lateral double-diffused MOS transistors (LDMOS) are merged with a BiCMOS process flow for the construction of power integrated circuits on bonded silicon-on-insulator (BSOI) substrates. All active and passive device structures have been optimized for fabrication on BSOI layers which are less than 1.5 mu m-thick, with buried oxide layers in the range of 2.0 to 3.0 mu m-thick. Complete dielectric isolation processing is straightforward due to the use of a thin SOI active device layer. A dual field plate design of the **high-voltage** devices results in at least a factor-of-two reduction in specific on-resistance

over conventional LDMOS structures for a given breakdown voltage. (Author abstract) 10 Refs.

7/3,AB/6 (Item 1 from file: 65)
DIALOG(R)File 65:Inside Conferences

04210125 INSIDE CONFERENCE ITEM ID: CN044168868
A thin-**layer high-voltage silicon**-on-insulator
hybrid LDMOS/LIGBT device
Petruzzello, J.; **Letavic, T.**; van Zwol, H.; **Simpson, M.**; Mukherjee, S.
CONFERENCE: International symposium on power semiconductor devices & ICs -14th
PROCEEDINGS OF THE INTERNATIONAL SYMPOSIUM ON POWER SEMICONDUCTOR DEVICES AND ICS-IEEE, 2002; 14TH P: 117-120
IEEE, 2002
ISBN: 0780373189
LANGUAGE: English DOCUMENT TYPE: Conference Papers and programme
CONFERENCE LOCATION: Santa Fe, NM 2002; Jun (200206) (200206)
NOTE:
IEEE cat no: 02CH37306

7/3,AB/7 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015544702
WPI Acc No: 2003-606858/200357
XRAM Acc No: C03-165191
XRPX Acc No: N03-483868
Dual gate oxide **high voltage semiconductor** device, e.g. lateral metal oxide **semiconductor** field effect transistor or diode, comprises second gate oxide formed over portion of first gate oxide
Patent Assignee: KONINK PHILIPS ELECTRONICS NV (PHIG)
Inventor: **LETAVIC T J; SIMPSON M R**
Number of Countries: 102 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030107087	A1	20030612	US 200115847	A	20011210	200357	B
WO 200350884	A1	20030619	WO 2002IB4895	A	20021120	200357	
AU 2002348845	A1	20030623	AU 2002348845	A	20021120	200420	

Priority Applications (No Type Date): US 200115847 A 20011210
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030107087	A1		7	H01L-031/62	
WO 200350884	A1	E		H01L-029/78	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SC SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VC VN YU ZA ZM ZW
Designated States (Regional): AT BE BG CH CY CZ DE DK EA EE ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SK SL SZ TR TZ UG ZM ZW

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
AU 2002348845	A1			H01L-029/78	Based on patent WO 200350884

Abstract (Basic): US 20030107087 A1

Abstract (Basic):
NOVELTY - A dual gate oxide **high voltage** **semiconductor** device (100) comprises a buried oxide layer formed over a **semiconductor** substrate (102), a **silicon layer** formed over the buried oxide layer (104), a top oxide **layer** formed over the **silicon layer**, a first gate oxide formed over the **silicon layer** adjacent the top oxide layer, and a second gate oxide formed over a portion of the first gate oxide.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method for forming a dual gate oxide **high voltage** **semiconductor** device.
USE - Used as **high voltage semiconductor** device e.g. lateral MOSFET or diode.
ADVANTAGE - Optimizes breakdown voltage and specific-on-resistance. Doping in the silicon can be increased without increasing the magnitude of the vertical electric field.
DESCRIPTION OF DRAWING(S) - The figure shows an enlarged view of a **semiconductor** device having dual gate oxide.
Semiconductor device (100)
Substrate (102)
Buried oxide layer (104)
Silicon layer (106)
Top oxide layer (114)
Field plate (116)
First gate oxide (124)
Second gate oxide (128)
pp; 7 DwgNo 3/3

7/3,AB/8 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015227885
WPI Acc No: 2003-288798/200328
XRPX Acc No: N03-229629
Hybrid **semiconductor** device for **high voltage** application, has MOSFET and diode which are relatively more and less resistant to breakdown voltage, respectively
Patent Assignee: KONINK PHILIPS ELECTRONICS NV (PHIG)
Inventor: **LETAVIC T J**; PETRUZZELLO J; **SIMPSON M R**; JAMES L T; JOHN P; MARK S
Number of Countries: 024 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030001209	A1	20030102	US 2001894083	A	20010628	200328	B
WO 200303464	A2	20030109	WO 2002IB2414	A	20020620	200353	
EP 1405348	A2	20040407	EP 2002735903	A	20020620	200425	
			WO 2002IB2414	A	20020620		

Priority Applications (No Type Date): US 2001894083 A 20010628
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030001209	A1		8	H01L-021/84	
WO 200303464	A2	E		H01L-027/12	

Designated States (National): CN JP KR
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1405348	A2	E		H01L-027/12	Based on patent WO 200303464

Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI

LU MC NL PT SE TR

Abstract (Basic): US 20030001209 A1

Abstract (Basic):

NOVELTY - The **semiconductor** device has MOSFET and diode which are relatively more and less resistant to breakdown voltage, respectively.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) method of constructing rugged transistor device;

(2) hybrid lateral thin **film silicon**-on-insulator device; and

(3) method of obviating bipolar second breakdown in MOS transistor.

USE - For **high voltage** application.

ADVANTAGE - Allows the device to survive any breakdown without being destroyed, resulting in a more rugged and more reliable silicon-on-insulator lateral drift metal oxide **semiconductor** (SOI-LDMOS) device.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the hybrid **semiconductor** device.

pp; 8 DwgNo 2/4

7/3,AB/9 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014419263

WPI Acc No: 2002-239966/200229

Related WPI Acc No: 1999-419182

XRPX Acc No: N02-185132

High voltage transistor for integrated circuits has initially wider drift region caused by offset doping profile and thinning of **semiconductor** on insulator layer

Patent Assignee: KONINK PHILIPS ELECTRONICS NV (PHIG); PHILIPS ELECTRONICS NORTH AMERICA CORP (PHIG)

Inventor: ARNOLD E; **LETAVIC T J**; **SIMPSON M R**; **LETAVIC T**; **SIMPSON M**

Number of Countries: 025 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200175980	A1	20011011	WO 2001EP3007	A	20010319	200229	B
US 6310378	B1	20011030	US 97998048	A	19971224	200229	
			US 2000539911	A	20000330		
KR 2002019047	A	20020309	KR 2001715312	A	20011129	200262	
EP 1269548	A1	20030102	EP 2001915360	A	20010319	200310	
			WO 2001EP3007	A	20010319		
TW 501266	A	20020901	TW 2001109915	A	20010425	200334	
CN 1422442	A	20030604	CN 2001801463	A	20010319	200356	
JP 2003529940	W	20031007	JP 2001573557	A	20010319	200370	
			WO 2001EP3007	A	20010319		

Priority Applications (No Type Date): US 2000539911 A 20000330; US 97998048 A 19971224

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200175980	A1	E	32	H01L-029/78	

Designated States (National): CN JP KR

Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR

US 6310378 B1 H01L-027/01 CIP of application US 97998048
KR 2002019047 A H01L-029/78
EP 1269548 A1 E H01L-029/78 Based on patent WO 200175980
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
TW 501266 A H01L-027/01
CN 1422442 A H01L-029/78
JP 2003529940 W 37 H01L-029/786 Based on patent WO 200175980

Abstract (Basic): WO 200175980 A1
Abstract (Basic):

NOVELTY - **Semiconductor** on insulator (SOI) device has doping profile and thinning of SOI layer offset allowing an segment (134) of the drift region (135) near the source (131) to be wider allowing greater current capacity.

DETAILED DESCRIPTION - An independent claim is also included for a method of fabricating the transistor. The substrate is topped by a **silicon layer** which has its resistance lowered with impurities. This is then appropriately treated with successive layers to form the transistor.

USE - Used as a **high voltage** transistor in integrated circuit devices.

ADVANTAGE - Transistor has improved current handling capability while maintaining an improved breakdown voltage capability.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section of the transistor.

Source region (131)
Offset region (134)
Drift region (135)
Drain region (136)
pp; 32 DwgNo 3/11

7/3,AB/10 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013933497
WPI Acc No: 2001-417711/200144
XRAM Acc No: C01-126198
XRPX Acc No: N01-309512

Thin-**film silicon**-on-insulator device, especially a **high-voltage** power device, comprises a lateral transistor and a lateral drift region having a retrograde doping profile with respect to buried and surface insulation regions

Patent Assignee: KONINK PHILIPS ELECTRONICS NV (PHIG); PHILIPS ELECTRONICS NORTH AMERICA CORP (PHIG)
Inventor: EGLOFF R; **LETAVIC T**; **SIMPSON M**; WARWICK A M
Number of Countries: 029 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200137346	A1	20010525	WO 2000EP10614	A	20001026	200144	B
US 6313489	B1	20011106	US 99440767	A	19991116	200170	
EP 1147561	A1	20011024	EP 2000979518	A	20001026	200171	
			WO 2000EP10614	A	20001026		
KR 2001101506	A	20011114	KR 2001708861	A	20010713	200230	
TW 472342	A	20020111	TW 2000124971	A	20001124	200281	
JP 2003514400	W	20030415	WO 2000EP10614	A	20001026	200328	
			JP 2001537800	A	20001026		

Priority Applications (No Type Date): US 99440767 A 19991116
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200137346	A1	E	14	H01L-029/78	

Designated States (National): JP KR
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6313489	B1			H01L-033/00	
EP 1147561	A1	E		H01L-029/78	Based on patent WO 200137346

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2001101506	A			H01L-027/12	
TW 472342	A			H01L-021/76	
JP 2003514400	W		17	H01L-021/336	Based on patent WO 200137346

Abstract (Basic): WO 200137346 A1
Abstract (Basic):

NOVELTY - Thin-**film silicon**-on-insulator (SOI) device comprises a lateral transistor and a lateral drift region having a retrograde doping profile with respect to buried and surface insulation regions

DETAILED DESCRIPTION - Lateral thin-**film silicon**-on-insulator (SOI) device includes substrate, buried insulating layer and lateral transistor formed in SOI layer on the buried insulating layer having a source of first type formed in a body region of second type. Lateral drift region of first type is adjacent the body region and forms lightly-doped drain region. Lateral drift region has retrograde doping profile between buried and surface insulation regions.

The doping at a portion of the lateral drift region adjacent the buried insulation layer is greater than that adjacent the surface insulation layer. A drain contact of first type is provided laterally spaced from the body region by the drift region.

USE - The silicon-on-insulator device is used in **high-voltage** power devices.

ADVANTAGE - The retrograde doping profile in the drift region increases breakdown voltage and reduces ON resistance.

DESCRIPTION OF DRAWING(S) - The drawing shows a lateral thin-film SOI device.

Semiconductor substrate (22)
Buried insulating layer (24)
SOI layer (26)
Source region (28)
Body region (30)
Lateral drift region (32)
Drain contact (34)
Surface insulation region. (38)
pp; 14 DwgNo 1/1

7/3,AB/11 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013240170
WPI Acc No: 2000-412044/200035
XRPX Acc No: N00-308014

Lateral thin **film silicon**-on-insulator device, e.g. MOSFET for **high-voltage** application, has lateral drift region with graded doping profile

Query/Command : prt max set

1 / 2 PLUSPAT - ©QUESTEL-ORBIT - image

PN	-	WO03050884 A1 20030619 [WO200350884]
TI	-	(A1) DUAL GATE OXIDE HIGH-VOLTAGE SEMICONDUCTOR DEVICE AND METHOD FOR FORMING THE SAME
OTI	-	(A1) DISPOSITIF SEMI-CONDUCTEUR A OXYDE HAUTE TENSION A DEUX GRILLES ET PROCEDE DE FABRICATION DE CE DERNIER
LA	-	ENGLISH (ENG)
PA	-	(A1) KONINKL PHILIPS ELECTRONICS NV (NL)
PA0	-	KONINKLIJKE PHILIPS ELECTRONICS N.V.; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL)
IN	-	(A1) SIMPSON MARK R; LETAVIC THEODORE J
AP	-	WOIB0204895 20021120 [2002WO-IB04895]
PR	-	US1584701 20011210 [2001US-0015847]
IC	-	(A1) H01L-029/423 H01L-029/78 H01L-029/786
EC	-	H01L-029/423D2B8 H01L-029/78B1 H01L-029/786B4B2
DS	-	AE; AG; AL; AM; AT; AU; AZ; BA; BB; BG; BR; BY; BZ; CA; CH; CN; CO; CR; CU; CZ; DE; DK; DM; DZ; EC; EE; ES; FI; GB; GD; GE; GH; GM; HR; HU; ID; IL; IN; IS; JP; KE; KG; KP; KR; KZ; LC; LK; LR; LS; LT; LU; LV; MA; MD; MG; MK; MN; MW; MX; MZ; NO; NZ; OM; PH; PL; PT; RO; RU; SC; SD; SE; SG; SI; SK; SL; TJ; TM; TN; TR; TT; TZ; UA; UG; UZ; VC; VN; YU; ZA; ZM; ZW; European patent (AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES; FI; FR; GB; GR; IE; IT; LU; MC; NL; PT; SE; SK; TR); OAPI patent (BF; BJ; CF; CG; CI; CM; GA; GN; GQ; GW; ML; MR; NE; SN; TD; TG); ARIPO patent (GH; GM; KE; LS; MW; MZ; SD; SL; SZ; TZ; UG; ZM; ZW); Eurasian patent (AM; AZ; BY; KG; KZ; MD; RU; TJ; TM)
DT	-	Corresponding document
CT	-	Cited in the search report US6310378(B1)(Cat. X);US6313489(B1)(Cat. X);US6028337(A)(Cat. X);US6023090(A)(Cat. X)
STG	-	(A1) Publ. Of int. Appl. With int. Search rep
AB	-	A dual gate oxide high-voltage semiconductor device and method for forming the same are provided. Specifically, a device formed according to the present invention includes a semiconductor substrate, a buried oxide layer formed over the substrate, a silicon layer formed over the buried oxide layer, and a top oxide layer formed over the silicon layer. Adjacent an edge of the top oxide layer, a dual gate oxide is formed. The dual gate oxide allows both specific-on-resistance and breakdown voltage of the device to be optimized.
UP	-	2003-26

2 / 2 PLUSPAT - ©QUESTEL-ORBIT - image

PN	-	US2003107087 A1 20030612 [US20030107087]

TI	-	(A1) DUAL GATE OXIDE HIGH-VOLTAGE SEMICONDUCTOR DEVICE
PA	-	(A1) KONINKL PHILIPS ELECTRONICS NV (US)
PA0	-	KONINKLIJKE PHILIPS ELECTRONICS N.V., [US]
IN	-	(A1) SIMPSON MARK R (US); LETAVIC THEODORE J (US)
AP	-	US1584701 20011210 [2001US-0015847]
PR	-	US1584701 20011210 [2001US-0015847]
IC	-	(A1) H01L-031/062
EC	-	H01L-029/423D2B8 H01L-029/78B1 H01L-029/786B4B2
PCL	-	ORIGINAL (O) : 257367000
DT	-	Basic
STG	-	(A1) Utility Patent Application published on or after January 2, 2001
AB	-	A dual gate oxide high-voltage semiconductor device and method for forming the same are provided. Specifically, a device formed according to the present invention includes a semiconductor substrate, a buried oxide layer formed over the substrate, a silicon layer formed over the buried oxide layer, and a top oxide layer formed over the silicon layer. Adjacent an edge of the top oxide layer, a dual gate oxide is formed. The dual gate oxide allows both specific-on-resistance and breakdown voltage of the device to be optimized.
UP	-	2003-25

INTERNATIONAL SEARCH REPORT

PCT/IB 02/04895

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L29/78 H01L29/786 H01L29/423

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

PAJ, EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 310 378 B1 (ARNOLD EMIL ET AL) 30 October 2001 (2001-10-30) figure 4	1-16
X	US 6 313 489 B1 (WARWICK ANDREW MARK ET AL) 6 November 2001 (2001-11-06) figure 1	1-8
X	US 6 028 337 A (SIMPSON MARK ET AL) 22 February 2000 (2000-02-22) figures 1,2	1-8
X	US 6 023 090 A (SIMPSON MARK ET AL) 8 February 2000 (2000-02-08) figure 1	1-8

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 February 2003	24/02/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Juhl, A

INTERNATIONAL SEARCH REPORT

patent family members

PCT/IB 02/04895

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			EP	1269548	A1	02-01-2003
			EP	0965145	A2	22-12-1999
			WO	9934449	A2	08-07-1999
			JP	2001513270	T	28-08-2001
			US	6346451	B1	12-02-2002
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			EP	1147561	A1	24-10-2001
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			EP	1044475	A2	18-10-2000
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			EP	1051757	A1	15-11-2000
			JP	2002532887	T	02-10-2002
			TW	439283	B	07-06-2001

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(e.g. EP1023455 or WO0133678)

Applications viewed: ...

European Patent Register

Date	Documents for publication number WO03050884	Procedure	Pages
2004-04-26	Info on entry into regional phase (pages 1-2)	Search/Exam	3
2004-04-14	1001-6E	Search/Exam	1
2004-04-14	EP1200 form in PDF format	Search/Exam	4
2003-12-19	Notification of the recording of a change	Search/Exam	1
2003-06-19	International publication pamphlet	Search/Exam	14
2003-06-19	Copy of the International Search report	Search/Exam	2
Date	Documents for publication number WO03050884	Procedure	Pages

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